Vertical NV-NEM Switches in CMOS Back-End-of-Line: First Experimental Demonstration and Array Programming Scheme

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***Abstract*—** Metallic interconnect layers in a standard 65 nm CMOS back-end-of-line (BEOL) process are leveraged to form vertically oriented non-volatile (NV) nano-electro-mechanical (NEM) switches for compact implementation of hybrid CMOS-NEM integrated circuits. A reconfigurable look-up table (LUT) implemented with an array of vertical NV-NEM switches is experimentally demonstrated. A row/column addressing scheme is proposed and demonstrated via simulation for programming an array of NV-NEM switches. Scaled NV-NEM technology is projected to be advantageous for high-speed (sub-10ns), low-power reconfigurable computing applications.

I. Introduction

In recent years, nano-electro-mechanical (NEM) switches have generated interest as an intriguing option for implementation of energy-efficient digital integrated circuits (ICs) [1]. This is because NEM switches offer the advantages of zero OFF-state leakage current, abrupt ON/OFF switching characteristics, non-volatility, and relatively low ON-state resistance. Monolithic integration of CMOS transistors and NEM switches can improve energy efficiency, which is especially important for Internet of Things (IoT) applications. To minimize the number of additional fabrication process steps, the metallic interconnect layers in a conventional CMOS back-end-of-line (BEOL) process can be leveraged to implement NEM switches [2],[3]. By vertically orienting the movable electrode in the NEM switches, their footprint is minimized [4], enabling high-density arrays of NEM switches.

Monolithic integration of CMOS transistors with non-volatile (NV) devices can enable "in-memory computing" (IMC) architectures to improve computational speed by eliminating the need for data transfer between a central processing unit (CPU) and memory. Resistive memory (ReRAM) arrays have extensively investigated to implement new IMC architectures [5] such as look-up tables (LUT). The higher (essentially infinite) set/reset resistance ratio of a NV-NEM switch makes it ideal for implementation of reconfigurable LUTs.

In this work, vertically oriented NV-NEM switches are implemented using multiple metallic interconnect layers in a standard 65 nm-generation CMOS BEOL process. A hybrid CMOS-NEM LUT is demonstrated. A row-column addressing scheme is presented for programming an array of NV-NEM switches, and computer simulations project that a scaled NV-NEM technology will be advantageous for high-speed, low-power reconfigurable computing applications.

II. Vertical NV-NEM Switch Fabrication

The NV-NEM switch has five terminals, as shown in Fig. 1: a movable beam, two actuation electrodes (Prog0/1) on either side of the movable beam, and two corresponding contact electrodes (D0/1). The movable beam is in the neutral (non-contacting) position as-fabricated. When a program voltage (V_{Prog}) is applied to actuation electrode Prog0, electrostatic force (F_{elec}) is generated between the beam and Prog0. If the voltage is greater than or equal to the pull-in voltage (V_{PI}), the beam will be actuated into contact with contact electrode D0; this is referred to as state "0" in this work. Alternatively, the beam can be programmed into state "1" by applying a program voltage to electrode Prog1.

Fig. 2 (a) shows a schematic cross-section of a vertical NV-NEM switch after typical 65 nm CMOS and BEOL metallization steps. The switch is fabricated using the bottom five metal and corresponding via layers to facilitate smaller contact gap for smaller programming voltage. The dielectric material around the beam must be selectively removed to allow for physical movement, *i.e.*, to release the beam. Fig. 2(b) shows the schematic cross-section after the release etch process.

In this work, CF_4-CHF_3-He plasma was used for the highly anisotropic release etch process. No additional lithography steps were employed. (Upper-level metal dummy structures were used to mask the etch process.) Fig. 3(a) shows a scanning electron microscope (SEM) image of the fabricated NV-NEM switch in the neutral state, where the movable beam is separated from the program and contact electrodes by air gaps. Fig. 3(b) shows the switch programmed in state "0." Fig. 3(c) shows the cross-section of the fabricated NV-NEM switch showing all the metal/ via structures from the interconnect layers. The contact electrodes, D0/1, are isolated from the corresponding program electrodes (Prog 0/1) by the intermetal dielectric (IMD) layer. The structural material for the electrodes and movable structure is copper with a thin outer layer of TaN liner. The non-volatility of the NEM switches is due to the contact adhesive force between metallic surfaces, *i.e.*, TaN-TaN contact: The switch is non-volatile when the spring restoring force of the movable beam (F_k) is smaller than the contact adhesive force between the beam and contact electrode (F_{adh}). Fig. 4 shows measured quasi-static current-voltage characteristics of a fabricated NV-NEM switch. The program voltage is ~25 V, matching simulation results obtained using Coventorware MEM+. Since the BEOL metal pitch is scaled down with advancements in CMOS process technology, the program voltage of BEOL NV-NEM switches will become compatible with CMOS I/O voltages at the 22 nm node and beyond [3].

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III. RECONFIGURABLE LOOK-UP TABLE

Fig. 5(a) illustrates the schematic diagram for a 2-bit input/1-bit output LUT implemented with an array of NV-NEM switches and gated CMOS buffers. It comprises a cross-point array with an input portion (on the left) and an output portion (on the right). The NV-NEM switches along a single column have shared contact electrodes D0 and D1. The NEM switches within a column also share Prog0 and Prog1 electrodes, which are used to program each NV-NEM switch via electrostatic actuation to bring it into physical contact with either an I/O0 electrode or an I/O1 electrode. The program electrodes are not shown in Fig. 5(a) for simplicity.

The number of rows in the array corresponds to the number of possible input combinations, *i.e.* address words ($=2^N$). Each combination of input bits and its corresponding truth table output (as shown in Fig 5(b)) is programmed by grounding one input bit line IBL or output bit line OBL at a time to program the vertical switches in one row at a time, and then applying a programming voltage (V_{Prog}) to the appropriate program electrode, so that programmed states reflect the truth table. Each IBL is connected to the corresponding OBL via a gated CMOS buffer [6], as shown in Fig. 5(b). The IBL corresponding to the selected address row stays low while the other IBLs are pulled high. For example, the input "10" pulls-up all the input bit lines except IBL_2, which corresponds to the address word 10, as seen in the voltage waveforms in Fig. 6. All OBLs are pre-charged high before the read operation. The read enable signal is driven high to propagate the states of IBLs to OBLs; only one OBL is pulled low which discharges an output line to read out the stored answer, as also shown in Fig. 6. A PN diode is introduced in series with each movable beam to prevent reverse leakage paths in the cross-point array that can result in a readout error due to bit lines discharging through an input NV-NEM switch [6].

The NV-NEM switch contributes a relatively small contact resistance to the readout signal path [2], so the intrinsic readout delay should be small. In this work the readout delay is dominated by the large parasitic capacitances associated with the probe pads and the relatively high on-state resistances and parasitic capacitances of the Gated CMOS Buffer (GCB) and diodes. These delays were verified by characterizing standalone GCB and diodes. The readout operation uses $V_{DD} = 1.2V$, which is appropriate for 65 nm CMOS devices.

IV. NV-NEM ARRAY PROGRAMMING SCHEME

A crossbar array addressing scheme can be used to lower the number of control lines from $2N^2$ to 2N. We propose herein a row/column-interchangeable half-select programming scheme to program individual NV-NEM switches in an array, extended from previous work [7], [8]. The NV-NEM switches are grouped into blocks each comprising a pair, as illustrated in Fig. 7. Each pair of switches shares one of their actuation electrodes, Prog1, which is connected to a row line. The Prog0 electrodes on the outside of the block are simply joined to the column lines. This block can be replicated to scale up the array to an arbitrarily large number of switches.

During a hold operation, each of the actuation (Prog0 and Prog1) electrodes is biased at a *hold* voltage (V_{hold}) as shown in the schematic in Fig. 8. Programming of a NV-NEM switch is achieved by increasing the electrostatic attraction between the desired actuation electrode and the movable beam. To prevent other switches along the same column from being unintentionally programmed or *set*, the voltage increment (V_{set+}) applied to the actuation electrode is not sufficient by itself to set the switch. The voltage on the opposite actuation electrode of the NV-NEM switch to be set is simultaneously reduced (by V_{set-}) to allow the net electrostatic force to be sufficient to set it. Fig. 8 illustrates the programming of a NV-NEM switch to state "0", *i.e.*, a Set-0 operation: Column 0 drives the Prog0 voltage above V_{hold} by V_{set+}, while Row 0 drives the Prog1 voltage to V_{set-} below V_{hold}, so that the beam pulls in to contact electrode D0. To *reset* a NV-NEM switch to the neutral state, a similar scheme is used except with a shorter programming pulse width. Multiple switches along a programming line can be set at the same time by applying the required set pulses to the complementary program lines. Fig. 9 shows 3-dimensional device simulation results for a 2×2 array of NV-NEM switches with feature sizes corresponding to 5 nm process technology (Table I).

Fig. 10 shows a timing diagram for simulated sequential set/reset operations. The sequence is as follows: switch (0,0) is set to state "0"; switch (1,0) is set to state "1"; switches (1,1) and (0,1) are simultaneously set to state "1"; switch (0,0) is reset to neutral state; switches (1,1) and (0,1) are reset; and finally switches (1,1) and (0,1) are set to state "0". From the beam displacement plots, set time of 11.8 ns and reset time of 6.14 ns are demonstrated.

Table II benchmarks the vertical NEM switches in 5nm node against SRAM technology in terms of performance parameters. The footprint of vertical NEM switch is 0.0104 μm^2, which is half the size of the state-of-the-art SRAM cell in 5nm node [10]. While the cell read energies are comparable, the cell write energy for the vertical NEM relay is a lot lower. This makes the NEM switches a good candidate for embedded NV memory.

V. CONCLUSION

Non-volatile (NV) vertically oriented nano-electro-mechanical (NEM) switches are successfully implemented for the first time using multiple back-end-of-line layers in a conventional 65 nm CMOS process, and used to demonstrate a hybrid CMOS-NEM look-up table (LUT). With technology scaling, NV-NEM technology compares favorably against conventional embedded memory technologies in terms of cell area, program/read speed and energy, showing promise for future embedded memory applications.

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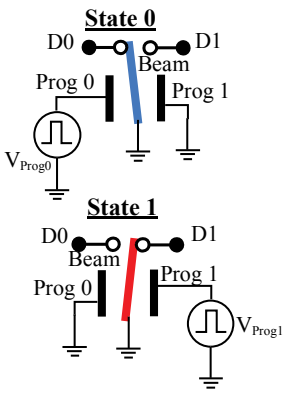

Fig. 1. Schematic illustrating programming operation of a vertical NEM switch to state "0" and state "1".

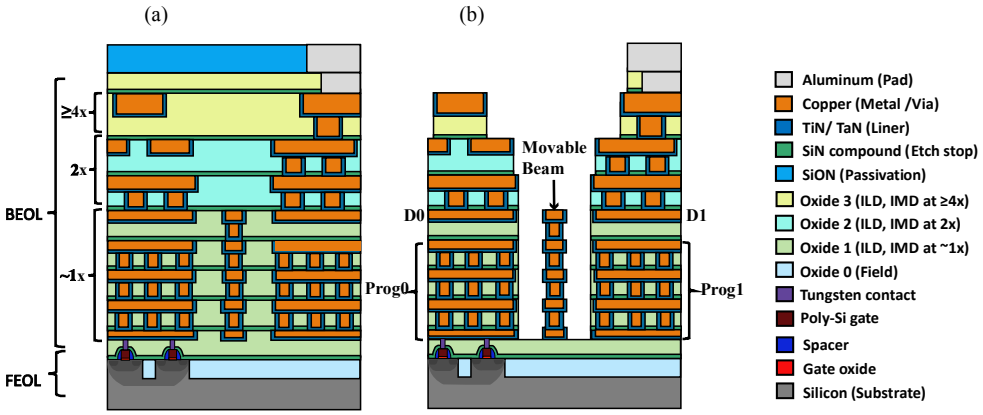

Fig. 2. Schematic cross-section illustrating the release etch scheme for a vertical NEM switch showing (a) the vertical switch and corresponding BEOL metallic interconnect layers after standard CMOS and BEOL fabrication and (b) after anisotropic release etch process. BEOL interconnect layers, including metal and via layers, inter-metal dielectric (IMD) and intra-layer dielectric (ILD) layers are shown.

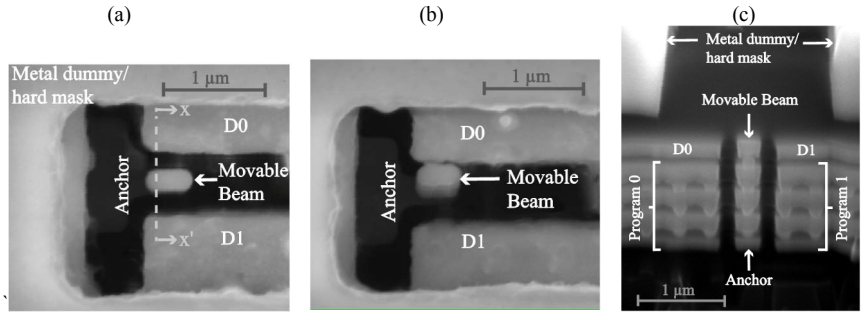

Fig. 3. Scanning Electron Microscope (SEM) images of fabricated vertical NEM switch showing (a) plan view of as-fabricated neutral state, (b) plan view of programmed switch in state "1", and (c) cross-sectional view along cutline x-x' after standard CMOS and BEOL fabrication.

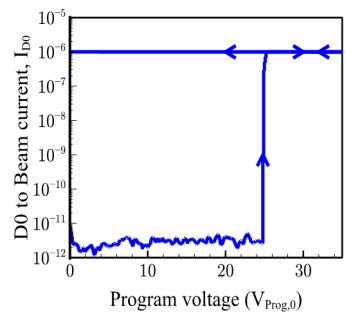

Fig. 4. Quasi-static current-voltage characteristics of a fabricated NV-NEM switch programmed to state "0". The current through D0 terminal is artificially limited to 1µA to avoid contact degradation due to Joule heating.

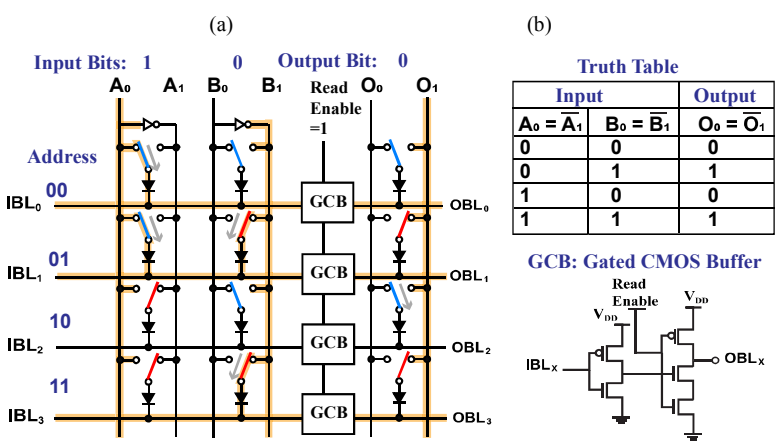

Fig. 5. Schematic of a 2-input/1-output look-up table (LUT), based on non-volatile vertical NEM switches. (a) Input bits "10" are used to address the array and an output bit of 0 is readout. The highlighted lines maintain a voltage of V_{DD} during readout. (b) Truth table for the LUT, and the gated CMOS buffer used to discharge the output bit line, OBL.

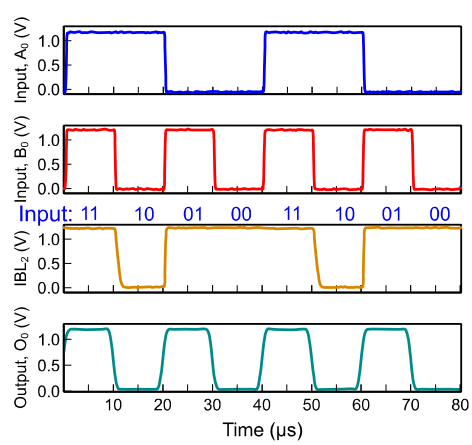

Fig. 6. Measured voltage waveforms demonstrating the operation of the 2 input-1 output look-up table (LUT). The read enable signal is kept high. Voltage waveform of input bit line IBL_2 is shown. Output O_0 reflects the truth table in Fig. 5(b).

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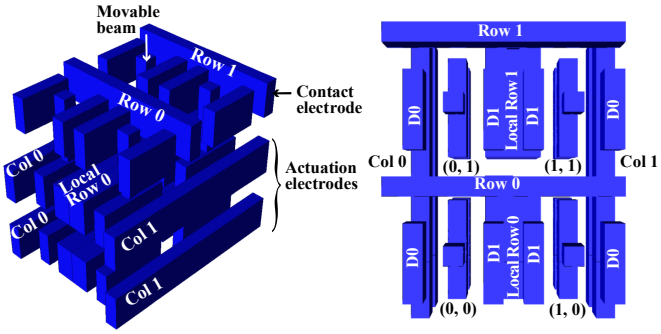

Fig. 7. (a) A 3D model of a 2x2 array of vertical NEM switches shown in neutral state, (b) top view the same array.

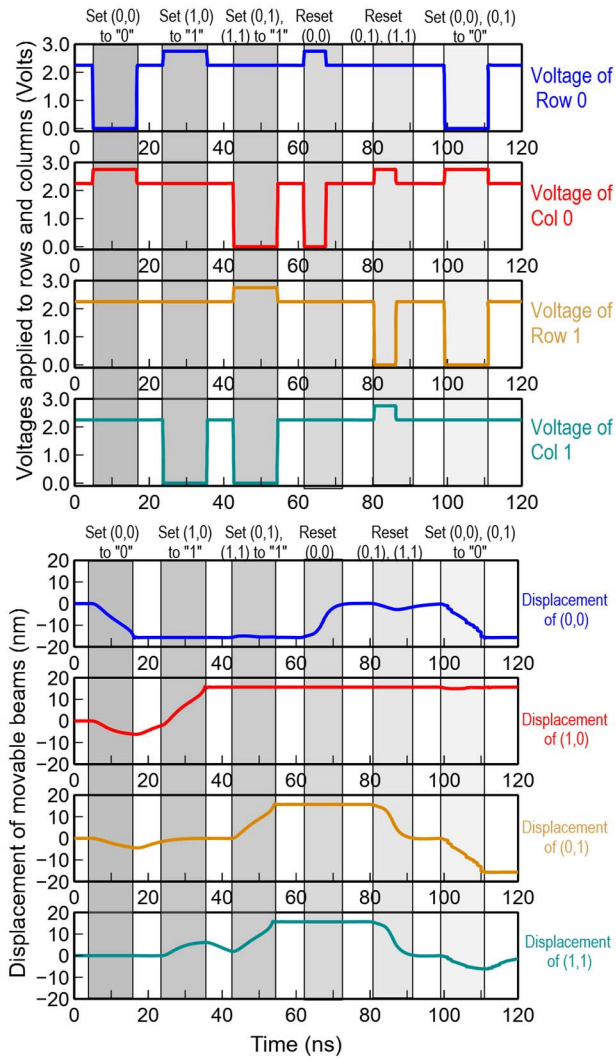

Fig. 10. Timing diagram for programming of a 2x2 non-volatile switch array.

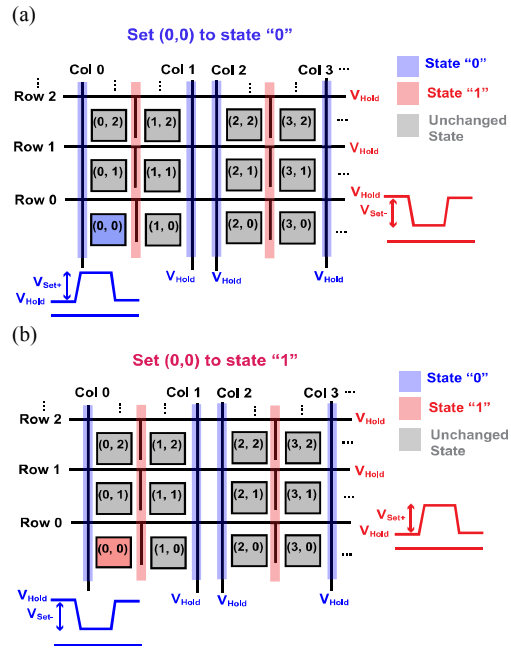

Fig. 8. Schematic showing (a) set to state "0" operation and (b) set to state "1" operation for switch (0,0) in a 3x4 array of NV NEM switches.

Table I. Design parameters used in the simulation in this work, based on 5nm technology node. Minimum pitch is close to values used in [8].

Design Parameter	Specifications/ Values
Technology node	5nm
Metal layers used for Prog0/1	M1-M2
Metal layer used for contact	M3
Metal/ via material	Copper
Minimum metal pitch	30nm
Minimum metal/via width	15nm
Beam-contact gap size	15nm
Beam-prog gap size	15nm
Contact area	840nm^2

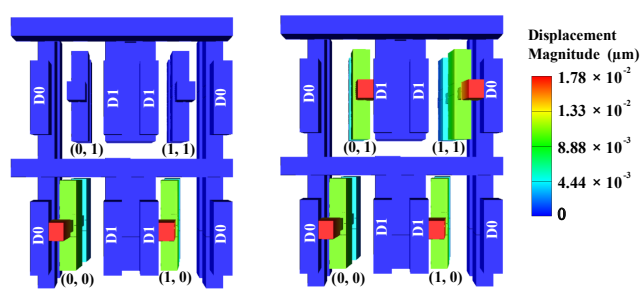

Fig. 9. 3D simulation results obtained from Coventorware MEMS+ showing a 2x2 array of vertical NEM switches with (a) switches (0,0) and (1,0) set to states "0" and "1" respectively, and (b) all the switches set to different states.

Table II. Performance benchmarking of vertical NEM switches against SRAM technology.

Design Parameter	Bit cell size	Write energy	Write delay	Read energy	Read delay
Vertical NEM Switch	~46 F^2 [This work]	~ 20 aJ [This work]	11.8 ns [This work]	<1pJ [6]	<1ns [6]
SRAM	>100 F^2	< 100 fJ	< 50ps	<1pJ	< 50 ps

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