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Evaporated tellurium thin films for p-type field-effect transistors and circuits

Chunsong Zhao[1,2,3,5], Chaoliang Tan[1,2,5], Der-Hsien Lien[1,2], Xiaohui Song[3,4], Matin Amani[1,2], Mark Hettick[1,2], Hnin Yin Yin Nyein[1,2,3], Zhen Yuan[1,2], Lu Li[1,2], Mary C. Scott[3,4] and Ali Javey[1,2*]

There is an emerging need for semiconductors that can be processed at near ambient temperature with high mobility and device performance. Although multiple n-type options have been identified, the development of their p-type counterparts remains limited. Here, we report the realization of tellurium thin films through thermal evaporation at cryogenic temperatures for fabrication of high-performance wafer-scale p-type field-effect transistors. We achieve an effective hole mobility of ~35 $cm^2V^{-1}s^{-1}$, on/off current ratio of ~10^4 and subthreshold swing of 108 mV dec^{-1} on an 8-nm-thick film. High-performance tellurium p-type field-effect transistors are fabricated on a wide range of substrates including glass and plastic, further demonstrating the broad applicability of this material. Significantly, three-dimensional circuits are demonstrated by integrating multi-layered transistors on a single chip using sequential lithography, deposition and lift-off processes. Finally, various functional logic gates and circuits are demonstrated.

Exploring semiconductor thin films grown at low temperature (400 °C or lower) with high mobility and device performance is of great importance for a number of applications including transparent/flexible electronics and monolithic three-dimensional (3D) complementary metal-oxide-semiconductor (CMOS) architectures[1–3]. Specifically, the processing temperature for constructing monolithic 3D CMOS, where multiple active circuit layers are stacked on top of each other, needs to be maintained below 300–400 °C to prevent degradation of the underlying devices and interconnects, and it needs to be even lower (below 200 °C or even less) for flexible electronics because of the low glass transition temperatures of polymer substrates (for example, the maximum stable temperature of polyethylene terephthalate (PET) is around 150 °C)[4–6]. Multiple n-type material systems with respectable electron mobility of the order of 10 $cm^2V^{-1}s^{-1}$, such as *a*-IGZO (amorphous indium gallium zinc oxide), zinc oxide, indium oxide, cadmium sulfide and cadmium selenide[1,7–10], have been identified, but the development of their p-type counterparts has been limited despite many years of effort. Widely explored low-temperature processing p-type thin films are amorphous silicon, metal oxides (for example, copper oxide, nickel oxide and tin oxide), organic compounds/polymers and polycrystalline germanium (Ge)[2,3,11,12]. Among them, amorphous silicon, metal oxides and organic compounds/polymers normally exhibit low hole mobilities of the order of 1 $cm^2V^{-1}s^{-1}$ or even less[2,5,11,13,14]. Vapour-phase-deposited polycrystalline germanium films give high hole mobility up to 110 $cm^2V^{-1}s^{-1}$. However, their applications are limited by the need for sequential annealing and/or metal catalysts to induce the crystallization[12]. Alternatively, carbon nanotubes (CNTs) have been explored as a promising p-type nanomaterial and solution-processed CNT-based networks exhibit hole mobility of up to tens of $cm^2V^{-1}s^{-1}$. However, their nanoscale processing remains a concern[6,15–18]. In addition, layer transfer of high-temperature grown materials such as chemical-vapour-deposition-grown CNT arrays and III–V compound semiconductors has also been explored, but large-scale processing necessary is still a challenge[4,19,20].

Recently, single-crystalline tellurium (Te) nanostructures with a bandgap energy of $E_g = 0.31$ eV have been shown to exhibit high hole mobilities up to 707 $cm^2V^{-1}s^{-1}$, but their large-scale processing is challenging, which hence limits their applications[21,22]. On the other hand, large-scale polycrystalline Te thin films with tens of nanometre thickness prepared by thermal evaporation were studied in the 1960–70s[23–25]. Material quality (that is, grain size) and transport properties (that is, carrier mobility) of the evaporated Te films were shown to be tuned by substrate temperature[24], nucleation layer[26,27] and deposition rate[26,27]. Specifically, the grain size strongly depends on the deposition temperature with the maximum size obtained at cryogenic temperatures[24]. Optimized evaporated Te films have shown high Hall mobility (up to a few hundred $cm^2V^{-1}s^{-1}$)[23,24]. However, high-performance field-effect transistors (FETs) with good switching characteristics have still not been achieved[23,25]. Here we report ultrathin Te thin films, which are deposited by thermal evaporation at low temperature (−80 °C), for fabrication of high-performance wafer-scale p-FETs, logic gates and computational circuits. The low processing temperature of Te p-FETs makes them compatible with a wide range of substrates, including silicon integrated circuits, glass and plastics.

Te thin-film synthesis and characterization

Te is composed of covalently bonded atoms sequenced in a helical chain along a single axis, with chains packed in a hexagonal array via van der Waals force (Fig. 1a). Domains with different contrast were observed under polarized light microscopy. The domains correspond to the arrays of aligned Te molecular chains, acting like wire grid polarizers, with absorption dependent on the angle between the light polarization and the array (polarized transmission measurements of different domains are shown in Supplementary Fig. 1). From X-ray diffraction (XRD) analysis, the absence of the (003) peak indicates that Te molecular chains are aligned in the plane of the substrate (Supplementary Fig. 2a). To further confirm the crystal structure of different domains, transmission electron

[1]Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, USA. [2]Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, CA, USA. [3]Department of Materials Science and Engineering, University of California at Berkeley, Berkeley, CA, USA. [4]The Molecular Foundry, Lawrence Berkeley National Laboratory, Berkeley, CA, USA. [5]These authors contributed equally: Chunsong Zhao, Chaoliang Tan. *e-mail: ajavey@eecs.berkeley.edu

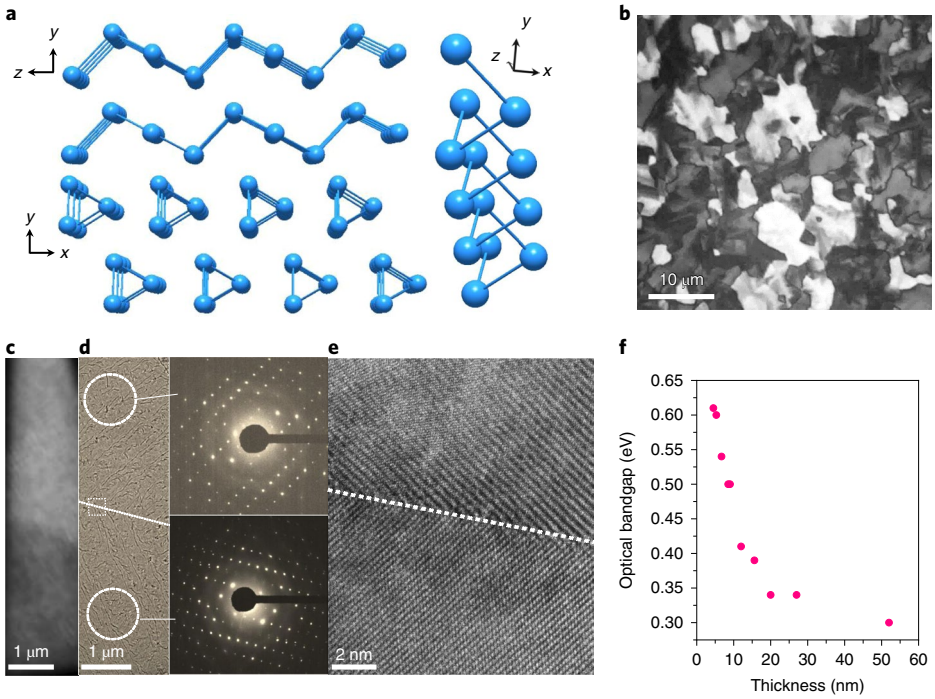

Fig. 1 | Characterization of Te thin films evaporated with a substrate temperature of −80 °C. a, Crystal structure of Te. **b**, Polarized light microscopy image of a Te film (9 nm). **c**, Enlarged optical image of a Te film (9 nm) on SiO_2 TEM grid, depicting a grain boundary. **d**, The low magnification TEM image of the Te film (9 nm) in **c**. The dashed line indicates the grain boundary. Insets are the corresponding selected-area electron diffraction patterns. **e**, HRTEM image of the same film at the boundary area. **f**, Thickness-dependent optical bandgap of Te thin films.

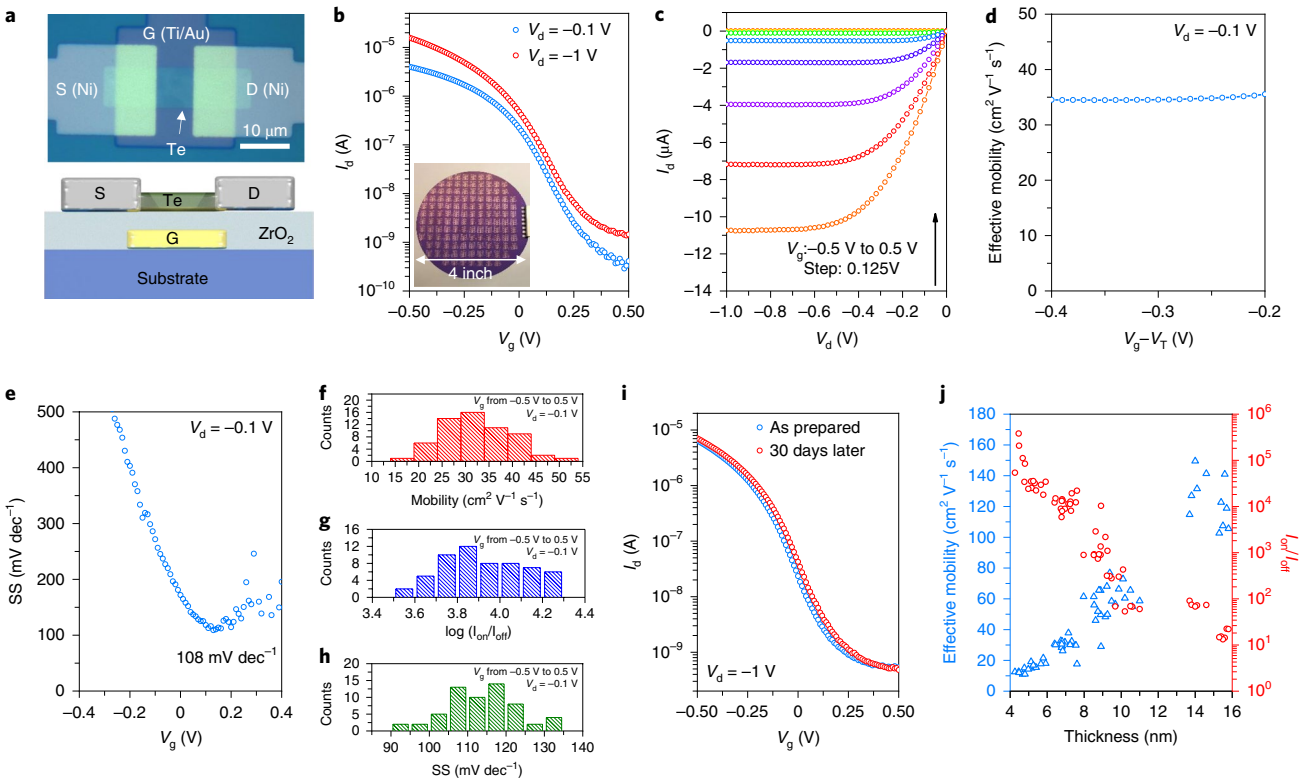

Fig. 2 | FETs based on Te evaporated with a substrate temperature of −80 °C. a, Optical image of a typical Te FET and schematic diagram of the device structure. **b**, I_d–V_g transfer curves of the Te transistor (8 nm) in **a**. Inset: photograph of wafer-scale (4-inch) Te FETs. **c**, I_d–V_d output characteristics of the same device as shown in **b**. **d**,**e**, Effective mobility (**d**) and SS (**e**) derived from the I_d–V_g curves shown in **b**. **f**–**h**, The statistical distribution of effective mobility (**f**), log (I_{on}/I_{off}) (**g**) and SS (**h**) for 60 individual transistors from different points on the wafer. **i**, I_d–V_g characteristic of a Te FET measured immediately and 30 days after fabrication. **j**, Thickness-dependent effective mobility (blue) and on/off current ratio (red) for Te FETs. Note that the thicknesses of Te film were measured by AFM.

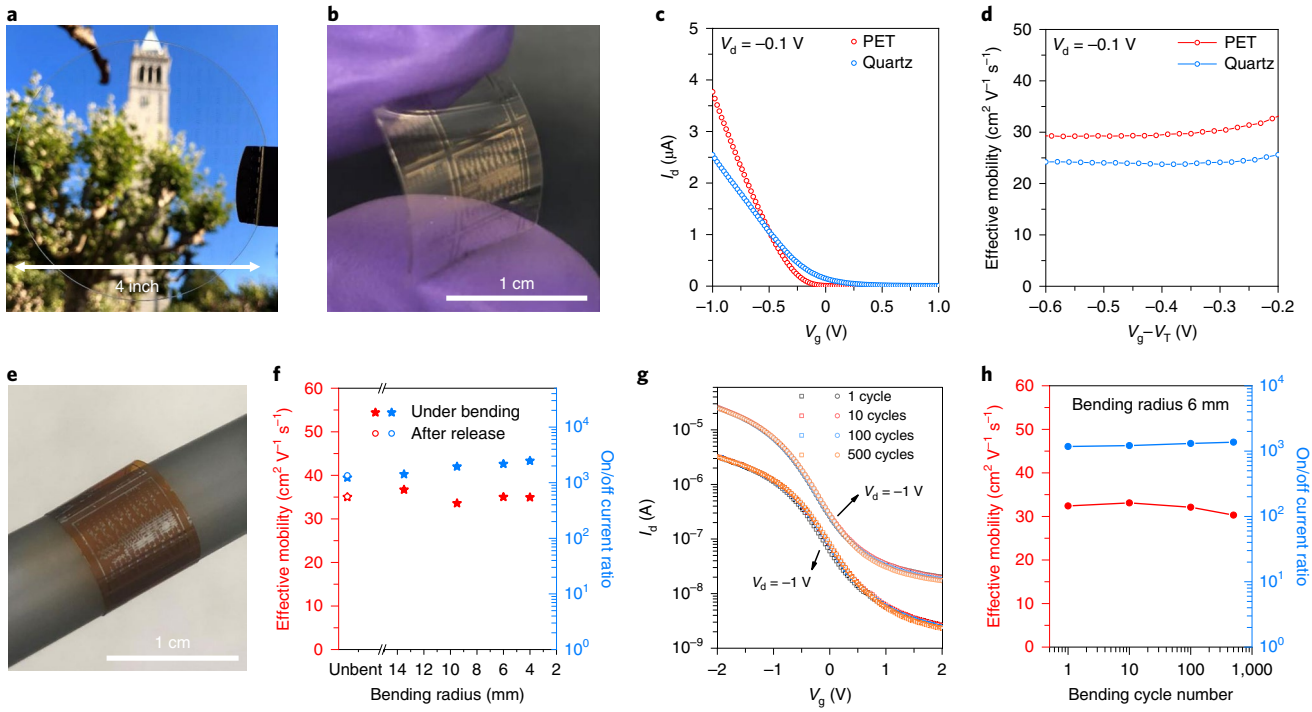

Fig. 3 | Flexible and transparent FETs based on Te evaporated with a substrate temperature of −80 °C. a,**b**, Photograph of Te FETs fabricated on 4-inch quartz wafer (**a**) and PET substrate (**b**). **c**, I_d–V_g transfer curves for evaporated Te FETs on quartz and PET substrates. **d**, Effective mobility of 8-nm-thick Te FETs on quartz and PET substrates. **e**, Photograph of Te FETs on Kapton substrate while bent (the thickness of the Kapton substrate is 50 μm). **f**, Effective mobility and on/off current ratio of Te FET (8 nm) on Kapton substrate under different bending radius. **g**, I_d–V_g transfer curves of the Te transistor (8 nm) on PET substrate after different bending cycles. **h**, Effective mobility and on/off current ratio of Te FET (8 nm) on Kapton substrate after different bending cycles.

microscopy (TEM) was performed (Fig. 1c). The selected-area electron diffraction patterns of two regions with different contrast show single-crystalline diffraction spots with different orientations, suggesting that both regions are single-crystal-like domains (Fig. 1d). The high-resolution (HR)TEM image clearly shows the grain boundary of the two domains (Fig. 1e). Note that defects can be observed from the HRTEM image (Supplementary Fig. 2b), suggesting that domains are not perfect single crystals.

We first investigate the thickness effect on the domain size of Te films evaporated with a substrate temperature of −80 °C. Te films with thickness varying from 8 to 30 nm were analysed using the polarized light microscope. We observed minimal thickness dependence for the domain size for the studied thickness of 8 to 30 nm (Supplementary Fig. 3). The extracted optical bandgap from the absorption measurements shows a thickness-dependent behaviour, from 0.3 eV for bulk to 0.6 eV for 4.5-nm-thick evaporated Te films (Fig. 1e and Supplementary Fig. 4) due to the quantum confinement effect. Our results are consistent with the previously reported calculations[28] and experimental results on single-crystalline Te layers[29].

We also found that the substrate temperature for evaporation has a significant impact on the Te film quality. When the substrate temperature decreases from −10 °C to −60 °C, the average area of domains monotonically increases from ~3 μm^2 to ~25 μm^2 (Supplementary Fig. 5). Below −60 °C, the domain size does not change with further decrease of temperature (Supplementary Fig. 5f). At room temperature (the substrate temperature of 25 °C), the film is not continuous and instead consists of small nanoparticles (Supplementary Fig. 5e).

Electrical characterization of Te FETs

The evaporation temperature effect on the device performance of Te FETs is explored given its significant impact on the domain size. We fabricate FETs based on Te films (8 nm) evaporated at different temperatures from 25 °C to −80 °C. The device structure consists of a Ti/Au local bottom gate, a 5-nm ZrO_2 (dielectric constant ≈ 16) gate dielectric (Fig. 2a) and Ni as source/drain metal contacts. The energy band diagram of the device is shown in Supplementary Fig. 6a. As shown in Supplementary Fig. 6b, the effective mobility decreases from 35 to 10 cm^{2}V^{-1}s^{-1} with the increase of the substrate temperature. The higher mobility for FETs based on Te thin film evaporated at −80 °C can mainly be attributed to larger domain size, compared to those deposited at higher temperatures[24]. To this end, we use Te films evaporated with a substrate temperature of −80 °C for subsequent device and circuit fabrication.

Uniform Te FETs can be easily fabricated at wafer scale given the simplicity of the Te deposition (Fig. 2b, inset). The Te FET shows a typical p-type characteristic as shown in Fig. 2b,c. A hysteresis in the voltage sweep measurement is observed, which is a common behaviour for a thin-film device without encapsulation (Supplementary Fig. 6c,d). The transistor exhibits an effective hole mobility of ~35 cm^{2}V^{-1}s^{-1}, on/off current ratio of ~10^4 and subthreshold swing (SS) of 108 mV dec^{-1} at room temperature (Fig. 2d,e). To study the uniformity of Te FETs, we randomly measured 60 devices on a wafer. The devices exhibit a narrow distribution in performance with standard deviation of 32 ± 7 cm^{2}V^{-1}s^{-1} in mobility, 9,491 ± 4,765 in on/off current ratio and 114 ± 9 mV dec^{-1} in SS (Fig. 2f–h). Importantly, the performance of the Te FET did not show obvious degradation after leaving the device in ambient air without any encapsulation for 30 days (Fig. 2i). Temperature-dependent drain current (I_d)–gate voltage (V_g) transfer curves are measured to investigate the carrier scattering mechanisms (Supplementary Fig. 6e,f). The effective mobility is nearly independent of temperature from 77 K to 300 K (Supplementary Fig. 6g), suggesting that the mobility is limited by the grain boundary and

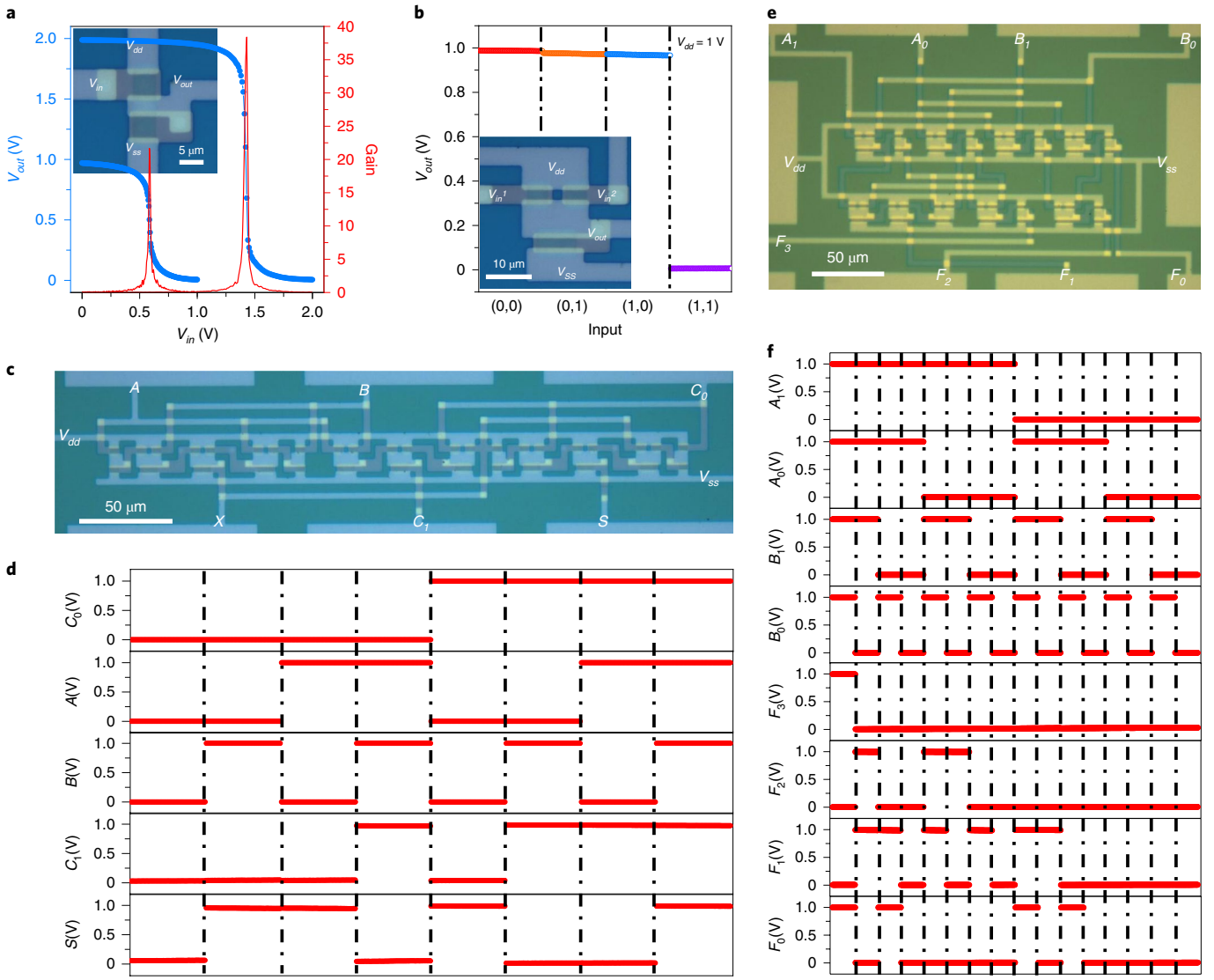

Fig. 4 | Integrated circuits based on Te FETs. a,**b**, Inverter (**a**) and NAND logic gate (**b**) performance. The inset shows an optical image of the device. **c**,**d**, Optical image (**c**) and output voltage (**d**) of a full-adder. **e**,**f**, Optical image (**e**) and output voltage (**f**) of a 2-bit multiplier. The supply voltage, V_{dd},was 1 V for the NAND gate, full-adder and 2-bit multiplier. Different input and the corresponding output states are separated by black dashed lines in **d** and **f**. Circuit designs and the experimental truth table are shown in Supplementary Fig. 9.

surface roughness scattering[22,30]. In the future, it may be possible to further improve the mobility by increasing the domain size and reducing the surface roughness by optimizing the evaporation process.

We then investigated the thickness-dependent effective mobility and on/off current ratio, which are the key metrics for transistors (Fig. 2j). Here, we vary the channel thickness from 4 to 16 nm. Te FETs become open circuits at sub-4-nm thickness and the evaporated films were found not to be continuous. The on/off current ratio decreases from ~10^5 (4 nm Te) to ~10 (16 nm Te), which is probably due to the decrase of the bandgap of the Te channel, and electrostatic control is reduced as thickness increases. In contrast, the effective mobility increases with thickness monotonically from 10 $cm^2V^{-1}s^{-1}$ to 140 $cm^2V^{-1}s^{-1}$. The monotonically increased mobility along with the film thickness could be attributed to the reduced effect of surface roughness scattering for thicker films, which is often observed in various material systems[19,31].

As a benefit of the low-temperature evaporation process, Te can be readily deposited on various substrates such as glass and plastic over large areas (Fig. 3a,b). We fabricated 8-nm-thick Te FETs on 4-inch quartz wafer and PET substrates with the same device structure shown in Fig. 2a. Te FETs on different substrates show similar hole mobilities (in the range of 25–35 $cm^2V^{-1}s^{-1}$) and on-state currents (Fig. 3c,d and Supplementary Fig. 7), suggesting that Te FETs can be used in broad applications, such as flexible and transparent electronics and displays[32]. We characterized the mechanical flexibility and operational stability of Te FETs on Kapton substrate. Fig. 3e shows a photograph of Te FETs on Kapton substrate when bent to a radius of 6 mm. The device mobility and on/off current ratio do not significantly change during bending up to a radius of 4 mm, corresponding to a tensile strain of 0.63% (Fig. 3f). A change in device performance is observed when strain is higher than 0.63%. The device becomes open circuit when strain reaches 1.5%, which is non-recoverable (Supplementary Fig. 8). Furthermore, the electrical properties of the device do not significantly change after multiple cycles (500) of bending at a radius of 6 mm, which corresponds to a strain of 0.42% (Fig. 3g,h).

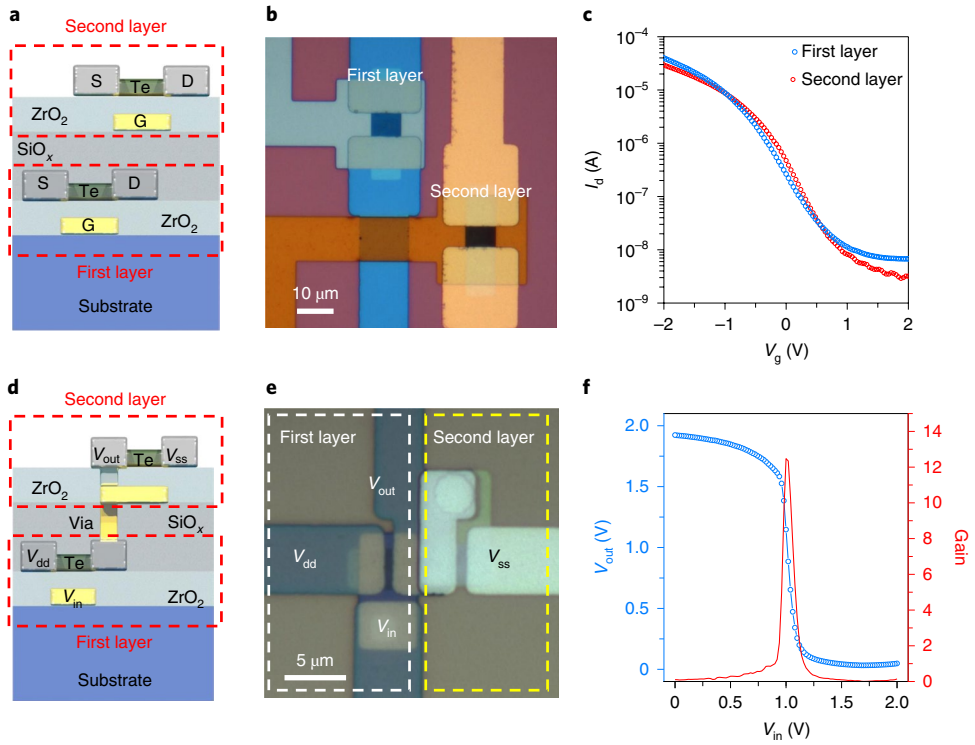

Fig. 5 | Multi-layered Te FETs and 3D inverters. a–c, A schematic diagram (**a**), optical image (**b**) and I_d–V_g transfer curves ($V_d = -1$ V) (**c**) of the two-layered transistor. The thickness of Te channels for both layers is 8 nm. **d–f**, A schematic diagram (**d**), optical image (**e**) and voltage transfer characteristic (**f**) of the 3D inverter based on Te FETs (with Te channels of 8 nm).

Logic gates and circuits based on Te devices

The high uniformity of Te FETs allows for fabrication of logic gates and computational circuits. Considering the trade-off between on/off current ratio and mobility, 8-nm-thick Te FETs are selected as the building blocks. First, a p-type metal-oxide-semiconductor (p-MOS) inverter, the simplest logic gate, is constructed using two Te devices, acting as the driver and active load, respectively (Fig. 4a inset and Supplementary Fig. 9a). Fig. 4a shows typical voltage transfer curves with a gain of 22 and 38 at an operating voltage $V_{dd} = 1$ V and $V_{dd} = 2$ V, respectively. We also fabricated a NAND gate with a logically valid output (Fig. 4b and Supplementary Fig. 9b). The basic logic gates facilitate the design of more complex circuits. A full-adder is a key component of arithmetic logic units, with myriad applications such as encoders, decoders and binary calculation[17]. Functionally, a full-adder is aimed to add two one-bit numbers (A and B) and one carry number (C_0), producing a two-bit sum (S) and new carry (C_1) as outputs. The Te FET based full-adder, which includes 9 NANDs and 4 inverters that are constructed from a total number of 35 transistors, is fabricated and shown in Fig. 4c. The full-adder functions properly with a maximum output voltage loss of 6% (Fig. 4c,d and Supplementary Fig. 9c,d). Therefore, we also fabricated a multiplier circuit to realize multiplication functions using 39 transistors. Functionally, four input terminals accept two 2-bit factors (A_1A_0 and B_1B_0) and the output is a 4-bit product ($F_3F_2F_1F_0$). The multiplication operation is achieved with a maximum output voltage loss of 3% (Fig. 4c,d and Supplementary Fig. 9e,f).

Demonstration of 3D monolithic circuits

The performance of Te p-FETs is sufficient to enable the realization of complementary 3D monolithic ICs and back-end-of-line electronics when combined with the existing n-FETs such as a-IGZO[1,4]. Therefore, as a proof-of-concept, we fabricated multilayer transistors and logic gates based on Te p-FETs. Figure 5a,b show the two-layer transistors fabricated using an evaporated SiO_x isolation layer. The devices on the first and second layers show similar I_d–V_g transfer curves (Fig. 5c). Importantly, the electrical property of the first layer does not significantly change after the construction of the top layer given the low processing temperature used for all the fabrication steps (Supplementary Fig. 10). Note that a small threshold voltage (V_t) shift is observed. This shift is probably caused by a fixed charge in the intermediate oxide or at the semiconductor–oxide interface, which can be improved by moving to a more suitable insulation layer or a more optimized deposition technique. A 3D circuit, specifically, a two-layer inverter, is also demonstrated. The upper-layer transistor, acting as an active load, is vertically connected to the bottom-layer transistor acting as the driver (Fig. 5d,f). The 3D inverter accomplishes the desired NOT function with a gain of approximately 12 at a $V_{dd} = 2$ V (Fig. 5f). These results demonstrate the practicality of Te p-FETs for monolithic 3D circuits.

Conclusions

We have demonstrated that evaporated Te thin films are an attractive material for p-FETs processed at low temperatures with important practical implications in monolithic 3D circuits, as well as flexible and transparent and/or large-area electronics. We believe that further improvements in the thin-film quality (for example, purity, crystallinity and surface smoothness) will enhance the device performance of Te FETs. Future integration of Te p-FETs with low-temperature n-type FETs, such as a-IGZO, can enable the construction of 3D CMOS circuits. Te p-FETs can also be implemented into back-end-of-line electronics with existing silicon CMOS circuits to further extend/enhance the system performance.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information,

acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41565-019-0585-9.

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Methods

Thermal evaporation of Te thin films. Te thin films were deposited in an Edwards Coating System (E306A thermal evaporator system) with a base pressure of about 1.5×10^{-6} mbar. Te pellets (99.999%, Sigma-Aldrich) were used as the thermal evaporation source. When the pressure reached 2×10^{-6} mbar, the substrate temperature was reduced to −80 °C by cooled nitrogen gas flow before the evaporation. The evaporation rate was controlled to be around 10 Å s^{-1} for all the evaporations. The thickness of Te thin film was monitored by during deposition. Following evaporation, the samples were taken out after the substrate temperature recovered to room temperature. All the Te thin films studied were prepared under these conditions, except for Te thin films evaporated at different substrate temperatures.

Device fabrication. *Single transistors.* FETs were fabricated on various substrates by the following photolithography, deposition and lift-off processes. First, gate regions were patterned on the SiO_2/Si, PET, Kapton or quartz substrates and Ti/Au (2 nm/18 nm) gate electrodes were deposited by electron-beam evaporation. The ZrO_2 dielectric layer was then deposited by atomic layer deposition (ALD). For single transistors on SiO_2/Si substrates, ZrO_2 was deposited at 200 °C with a thickness of 5 nm. For transistors on PET and quartz, ZrO_2 was deposited at 110 °C with a thickness of 10 nm. For transistors on Kapton, ZrO_2 was deposited at 110 °C with a thickness of 20 nm. Following the gate fabrication, Te channel regions were patterned over the gate area and Te was deposited. After the lift-off process, source and drain regions were patterned. Ni (30 nm) was deposited by electron-beam evaporation as metal contact. For Te FETs on quartz, sputtered indium tin oxide was used as gate (20 nm) and contact material (25 nm) to enable device transparency.

Logic gates and circuits. For the logic circuits a 10 nm ZrO_2 layer was deposited at 200 °C by ALD as the dielectric layer. Via regions were etched by buffered hydrofluoric acid (HF) solution. Additionally, Ni/Au (20 nm/10 nm) contacts were used to avoid Ni etching by buffered HF solution.

Two-layered transistors and 3D inverters. The bottom layers were fabricated using the process described above. After the fabrication of the bottom layer, 30 nm SiO_x was deposited on the top as an intermediate insulation layer by electron-beam evaporation and then the next layer was built on the top using the same procedure used for the first layer. ZrO_2 (10 nm) was deposited at 110 °C by ALD.

Characterizations. Te thin films with varying thickness were deposited on quartz substrates for the optical measurements. The thicknesses of Te thin films for optical bandgap measurements and thickness-dependent device performance were measured by atomic force microscope (AFM) (Dimension ICON AFM microscope (Bruker), operating in tapping mode). All other thickness measurements were based on the crystal quartz monitor. TEM characterization was performed on 9-nm-thick Te deposited on SiO_2 support TEM membrane (TED PELLA). The Te film in Fig. 1c was patterned and transferred on a SiO_2 support TEM membrane. TEM characterization was carried on an FEI Titan 60–300 microscope with an acceleration voltage of 200 kV at the National Center for Electron Microscopy at Lawrence Berkeley National Laboratory. The sample for XRD measurement was deposited on glass with a thickness of 50 nm (based on the quartz crystal monitor). XRD measurement was performed on an AXS D8 Discover GADDS, Bruker with a Co Kα X-ray source (wavelength $\lambda = 1.7903$ Å). A Shimadzu SolidSpec-3700 spectrometer was used to measure the transmission and diffuse reflection of the samples. The polarized light optical microscopy images of Te thin films were taken by a polarized LV100N optical microscope (Nikon). Room-temperature electrical measurements were performed in a probe station using a 4155C Semiconductor Parameter Analyzer (Agilent Technologies). Temperature-dependent electrical measurements were performed in a cryogenic probe station (LakeShore) with a B1500a Semiconductor Device Analyzer (Keysight). Effective mobility was calculated using

$$\mu_{\mathrm{eff}} = \frac{\mathrm{d}I_{\mathrm{d}}}{\mathrm{d}V_{\mathrm{d}}}\frac{L}{WC_{\mathrm{ox}}(V_{\mathrm{g}} - V_{\mathrm{t}})} \quad (1)$$

where C_{ox} is the gate oxide capacitance, L is the channel length, W is the device width and V_t is the threshold voltage. I_d was measured at low bias ($V_d = -0.1$ V). Subthreshold swing (SS) is derived from the equation

$$\mathrm{SS} = \left(\frac{\mathrm{d}(\log I_{\mathrm{d}})}{\mathrm{d}V_{\mathrm{g}}}\right)^{-1} \quad (2)$$

at the low bias ($V_d = -0.1$ V).

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author on reasonable request.

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Author contributions

C.Z., C.T. and A.J. conceived the idea for the project. C.Z. and A.J. designed the experiments. C.Z., M.A. and Z.Y. fabricated the devices. C.Z. performed the device measurements. C.Z., C.T., X.S., D.-H.L., M.H., H.Y.Y.N., L.L. and M.S. performed material characterizations. C.Z. and A.J analysed the data. C.Z., C.T., D.-H.L. and A.J. wrote the manuscript. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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Correspondence and requests for materials should be addressed to A.J.

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