Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications

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***Abstract*—**Operation of micro-electro-mechanical (MEM) relays at temperatures down to 4 K is demonstrated for the first time. Due to a dramatic reduction in hysteretic switching behavior and elimination of contact oxidation, MEM relays can be operated reliably with sub-25 mV voltage signals at temperatures below 100 K. This makes them advantageous for implementing ultra-low-power digital logic circuits for cryogenic applications such as quantum computing.

I. Introduction

Operation of digital logic circuitry at cryogenic temperatures is of growing interest due to the advent of quantum computers, which require electronic switches to manipulate and read individual quantum bits (qubits) [1]. Ideally, this electronic control circuitry should be monolithically integrated with the qubits and hence should dissipate as little energy as possible in order to maintain the computer at milli-Kelvin (mK) temperatures. In principle, metal-oxide-semiconductor field-effect transistors (MOSFETs) can operate at cryogenic temperatures with very small subthreshold swing (SS), which would allow a high on/off current ratio to be achieved with ultra-low (sub-100 mV) gate voltage swing. However, a recent experimental study has revealed that, due to temperature-dependent oxide-interface trap density, SS for conventional bulk-silicon MOSFETs operated at 4 K exceeds 10 mV/dec, which is well above the limit set by Boltzmann statistics [2]. In addition to small SS, transistors must have very small threshold voltages (well below 100 mV in magnitude) in order for complementary MOS (CMOS) digital logic circuitry to function with ultra-low supply voltage. This may be difficult to achieve in practice at cryogenic temperatures, due to dopant freeze-out effects. In contrast, micrometer-scale electro-mechanical (MEM) relays have been experimentally demonstrated to operate with zero off-state leakage and ultra-low switching voltage signals, enabling the demonstration of sub-50 mV digital integrated circuits at room temperature [3,4]. In this work, the operation of MEM relays and relay-based integrated circuits at temperatures down to 4 K is experimentally investigated for the first time.

II. Relay Fabrication and Operation

Fig. 1 is a scanning electron micrograph (SEM) image of a fabricated MEM relay, which comprises a movable gate electrode suspended by four folded-flexure beams over a fixed body electrode, and two pairs of source/drain electrodes. The schematic cross-sectional views in **Fig. 2** show the as-fabricated air gap between the two metal conductive (source and drain) electrodes, g_d, as well as the as-fabricated actuation gap g_o. When a voltage difference is applied between the gate and body, the electrostatic force due to the applied voltage (V_{GB}) will actuate the movable gate towards the body. This force is opposed by the spring restoring force of the folded flexure beams. The air gap g_o is designed to be larger than three times g_d so that the relay operates in non-pull-in mode. When the structure is actuated sufficiently to cause the source electrode to come into physical contact with the underlying drain electrode, current (I_{DS}) can flow between the source and drain under the influence of an applied voltage between drain and source (V_{DS}); this is defined as the on-state. The minimum value of V_{GB} that causes the relay to turn on is referred to herein as the turn-on voltage, V_{ON}. In the on-state, adhesive force exists between the source and drain electrodes. Therefore, to turn off the relay, the spring restoring force needs to exceed the sum of the adhesive force and the electrostatic force due to V_{GB}. The value of V_{GB} that is just small enough to cause the relay to turn off is referred to herein as the release voltage, V_{RL}. The difference between V_{ON} and V_{RL} is referred to as the hysteresis voltage, V_H. By applying a DC bias (V_B) to the body electrode such that $V_B = -V_{RL}$, the relay can be switched on and off by swinging the gate voltage (V_G) between 0 V and V_H. Therefore, decreasing V_H enables lower-voltage relay operation.

Conventional planar processing techniques are used to fabricate MEM relays, with a maximum substrate temperature below 450 °C for compatibility with post-CMOS (and post-qubit) integration. **Fig. 3** illustrates the key process steps. First, an 80 nm-thick electrically insulating Al_2O_3 layer is deposited by atomic layer deposition (ALD) on a silicon wafer substrate, then a 60 nm-thick tungsten (W) layer is deposited by DC-sputtering. Lithography and reactive ion etching (RIE) processes are performed to pattern the body electrodes, drain electrodes, and source anchors. Then a 160 nm-thick low-temperature deposited silicon dioxide (LTO) layer is deposited as a first sacrificial layer by low pressure chemical vapor deposition (LPCVD) at 400 °C with O_2 and SiH_4 as precursor gases. The source dimples are then defined by lithography and RIE to remove the LTO over the drain electrodes in the contact regions. Afterwards a second sacrificial layer of 60 nm-thick LTO is also deposited using the same LPCVD recipe. Note that the thickness of the second LTO layer corresponds to g_d, while the sum of the two LTO layers corresponds to g_o. Lithography and RIE processes are then applied to remove the LTO in regions over the source anchor electrode. The second layer of 60 nm-thick tungsten is then deposited and patterned to form the dimpled source electrodes above their respective drain electrodes and in contact with their respective source anchor electrodes. Afterwards, a second 55 nm-thick layer of Al_2O_3 is deposited by ALD. Lithography and RIE are then used to remove the second layer of Al_2O_3 and the LTO over the

structural anchor regions, exposing the underlying first tungsten layer. The structural layer consisting of 1.9 μm-thick boron-doped polycrystalline-$Si_{0.4}Ge_{0.6}$, is then deposited via LPCVD at 410 °C for 5 hours. A 400 nm-thick LTO hard-mask layer for patterning the structural layer is then deposited by LPCVD at 400 °C. Then the hard mask, structural, and Al_2O_3 layer stack is patterned by lithography and RIE, exposing the second LTO layer. Finally, vapor HF is used to selectively remove the sacrificial LTO while avoiding capillary-force-induced stiction.

III. Results and Discussion

In this work, the fabricated relays and circuits were tested under vacuum at temperatures from 4 K to 300 K. Relay I_{DS}-*vs*.-V_G characteristics are shown in **Fig. 4**. The relay switches on and off abruptly with sweeping gate voltage, and an applied body bias allows for low gate voltage operation. The hysteresis voltage is only 4 mV at 4 K, indicating that MEM relay circuits potentially can be operated with sub-10 mV voltage signals – roughly two orders of magnitude lower than MOSFETs.

Operation of a 2:1 relay-based multiplexer integrated circuit at 300 K and 77 K is shown in **Fig. 5**. Note that the upper relay has positive body bias (V_{BP}) so that it turns on when the select voltage signal (V_{SEL}) is low, while the lower relay has negative body bias (V_{BN}) so that it turns on in a complementary manner when V_{SEL} is high. Thus the upper relay will pass the voltage signal V_A to the output (*i.e*., $V_{OUT} = V_A$) when V_{SEL} is low (logic '0'), and the lower relay will pass the voltage signal V_B to the output (*i.e*., $V_{OUT} = V_B$) when V_{SEL} is high (logic '1'). The waveforms in **Fig. 5(c)** show proper circuit operation at 300 K with 100 mV signals, while the waveforms in **Fig. 5(d)** show proper circuit operation at 77 K with < 25 mV signals, made possible by smaller V_H values. (It should be noted that V_{OUT} was monitored by an oscilloscope with an internal impedance of 1 MΩ. If a relay has high on-state resistance (R_{ON}) – due to electrode surface oxide formation – the input voltage signal will not be fully passed to V_{OUT} due to the voltage divider effect.)

Measured temperature dependences of V_{ON} and V_H for a MEM relay are shown in **Figs. 6** and **7**, respectively. The slight increase in V_{ON} with decreasing temperature can be explained by an increase in structural stiffness, that is an increase in the Young's modulus of the poly-SiGe, with decreasing temperature. To confirm this mechanism, the natural resonant frequency (ω_0) of the structure is measured at 300 K, 77 K, and 4 K as shown in **Fig. 8**. A voltage slightly less than V_{ON} is applied to the gate and an applied V_{DS} provides the remaining electrostatic force (in the contact dimple region) to turn on the device. When the drain and source electrodes come into contact, the voltage difference between them is reduced, causing the relay to turn off; when the electrodes are separated, the voltage difference returns to V_{DS}, and so on, resulting in resonant frequency oscillation. Since $\omega_0 \propto \sqrt{k} \propto \sqrt{E}$ (where k is the composite stiffness of the folded-flexure suspension beams and E is the Young's modulus), it can be deduced that a decrease in temperature increases the Young's modulus. Interestingly, the hysteresis voltage decreases dramatically with decreasing temperature, indicating that the contact adhesive force diminishes with decreasing temperature [5].

Relays used for implementing digital logic must operate properly over many switching cycles to be of practical use. From previous studies, the primary reliability issue for MEM relays is contact oxidation causing the R_{ON} to increase dramatically over the lifetime of the device [6]. (Even in a vacuum environment with 1 μTorr pressure, trace amounts of O_2 lead to native oxide formation on the surfaces of the W electrode.) **Fig. 9** shows how R_{ON} depends on temperature, increasing significantly for temperatures above 90 K. Since 90 K is the boiling point of oxygen gas (O_2), sub-90 K operation inhibits the formation of native oxide on the electrode surfaces and thereby allows low R_{ON} to be maintained. **Fig. 10** compares how R_{ON} evolves over many on/off switching cycles using 5 kHz square-wave gate voltage signals with 2 V gate overdrive and V_{DS} = 0.5 V, at various temperatures. Considering that R_{ON} should not exceed 10 kΩ for acceptable relay-based integrated circuit performance [7], the (hot) switching endurance of a MEM relay operating at 300 K is roughly 10^6 cycles. For relays operated at liquid nitrogen temperature (77 K) or liquid helium temperature (4 K), however, the endurance of a relay exceeds 10^8 cycles, since there is no O_2 to oxidize the W electrodes.

Changes in electrical conductivity of the electrode materials were gauged by sheet resistance measurements of the contacting electrode layer (60 nm-thick W) and the structural gate electrode layer (1.9 μm-thick p-type poly-SiGe), as shown in **Fig. 11**. The poly-SiGe does not show dopant freeze-out effects down to 1.8 K, and the resistance of W also remains low, indicating that MEM relays can operate at temperatures as low as 1.8 K. **Fig. 12** shows measurements of relay turn-on delay at 300 K and 4 K. With a preset current compliance, the voltage across the source and drain decreases when the relay turns on; therefore, the time when the output voltage starts to drop corresponds to the time that the relay is turned on. The mechanical turn-on delay at 4 K (0.22 μs) is slightly worse than that at 300 K (0.19 μs), possibly due to increased damping coefficient and lower gate overdrive ratio (V_{GB}/V_{ON}).

IV. Conclusion

MEM logic relays operate with lower hysteresis voltage and stable on-state resistance at temperatures below 90 K, with endurance exceeding 10^8 switching cycles. Sub-25 mV relay circuit operation is demonstrated at cryogenic temperatures. Our experimental results indicate that relays should be able to operate properly at temperatures as low as 1.8 K, making them promising candidates for ultra-low-power cryogenic computing applications such as quantum computing.

Acknowledgments

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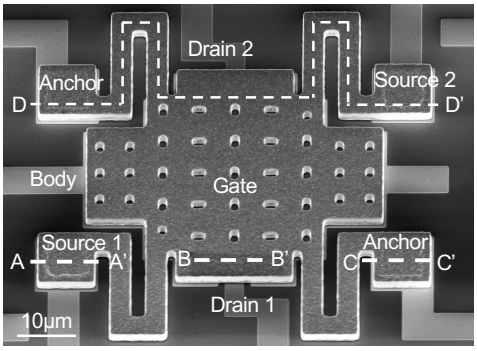


Fig. 1. 30° tilted SEM image of a MEM logic relay.

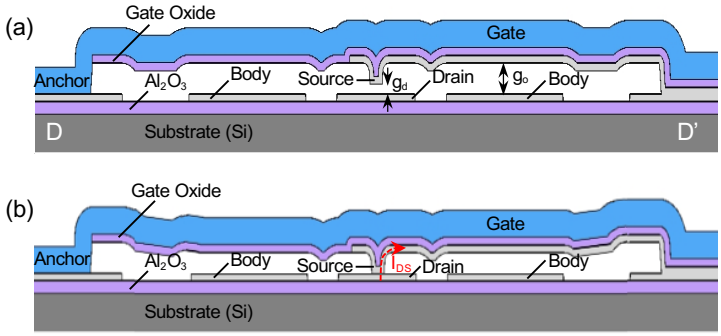


Fig. 2. Schematic cross-sectional views along D-D': (a) off-state (b) on-state.

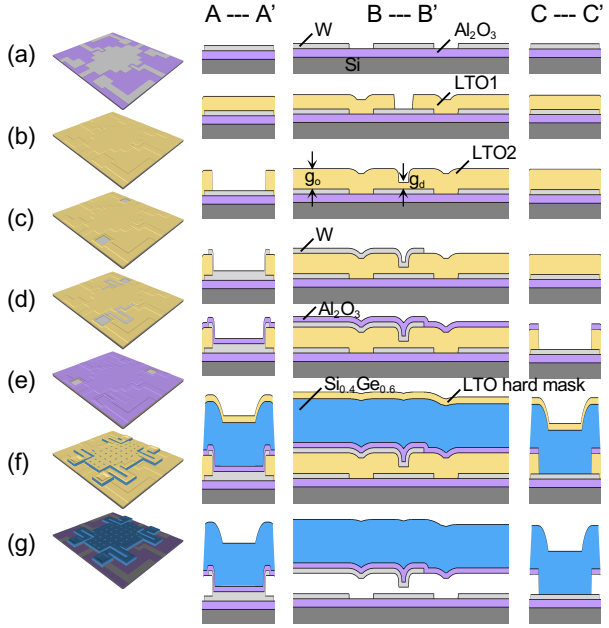


Fig. 3. Isometric and cross-sectional views along A-A', B-B', and C-C' (cf. Fig. 1) to illustrate the relay fabrication process: (a) Deposit and pattern the W electrodes on top of an Al_2O_3-coated Si substrate. (b) Deposit the first sacrificial low temperature deposited oxide (LTO) layer and define the contact regions. (c) Deposit and pattern the second sacrificial LTO layer (d) Deposit and pattern the second W layer to form the source electrodes. (e) Deposit and pattern the Al_2O_3 gate-insulating layer to expose the anchor regions. (f) Deposit and pattern SiGe structural layer. (g) Release in vapor HF.

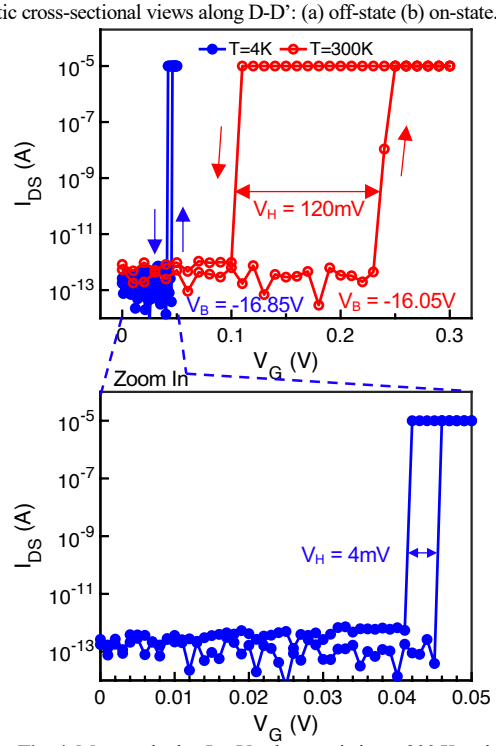
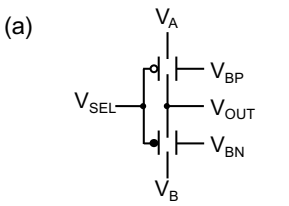


Fig. 4. Measured relay I_{DS}-V_G characteristics at 300 K and 4 K, under ~1 μTorr pressure. The gate voltage step size is 10 mV for 300 K, and 1 mV for 4 K. The current compliance limit was set to 10 μA.



(b)

V_{SEL}	V_{OUT}
0	V_A
1	V_B

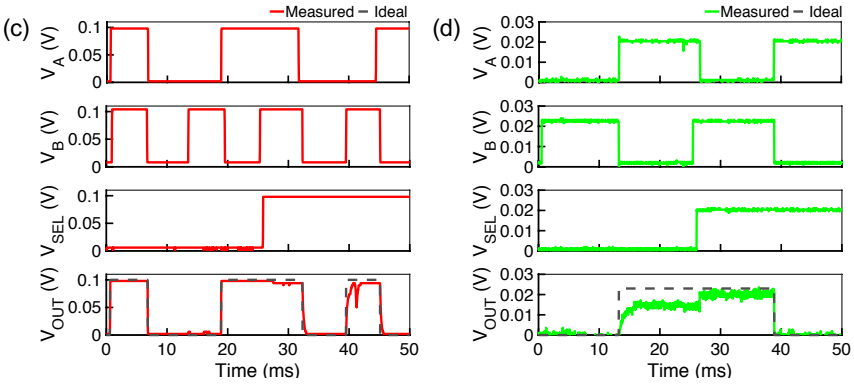


Fig. 5. Demonstration of ultra-low-voltage operation of a 2:1 multiplexer integrated circuit: (a) schematic circuit diagram and (b) truth table; measured voltage waveforms (c) at 300 K (V_{BP}=15.5 V, V_{BN}=-14.6 V) and (d) at 77 K (V_{BP}=17.07 V, V_{BN}=-14.71 V).

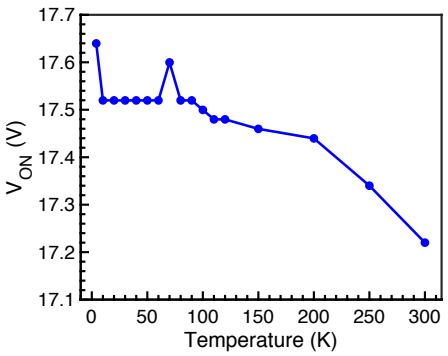


Fig. 6. Measured temperature dependence of V_{ON} for a single relay. V_{ON} increases slightly with decreasing temperature due to increased structural stiffness.

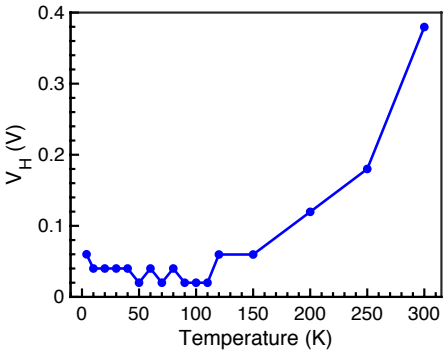


Fig. 7. Measured temperature dependence of V_H for a single relay. V_H decreases remarkably with decreasing temperature due to reduced contact adhesive force.

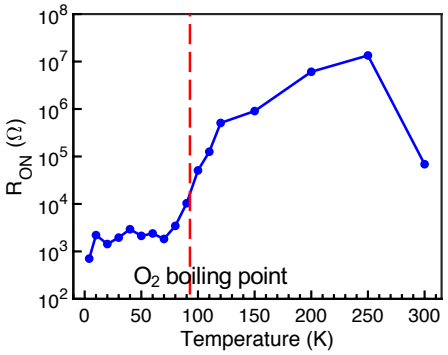


Fig. 9. Measured temperature dependence of R_{ON}. R_{ON} is fairly stable at temperatures below 90 K, and increases sharply when the temperature increases above 90 K, the boiling point of oxygen gas. At 300 K it is likely that the native oxide formed on the surface of the W electrodes broke down during the DC switching measurement, causing R_{ON} to be diminished.

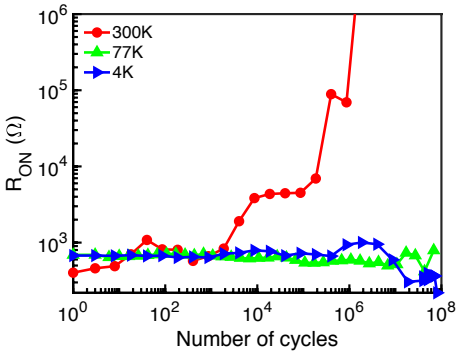


Fig. 10. Stability of R_{ON} over many on/off switching cycles with 5 kHz square-wave gate voltage signals, measured at 4 K, 77 K, and 300 K. R_{ON} remains low over 10^8 switching cycles when the operating temperature is below 90 K, due to the lack of O_2.

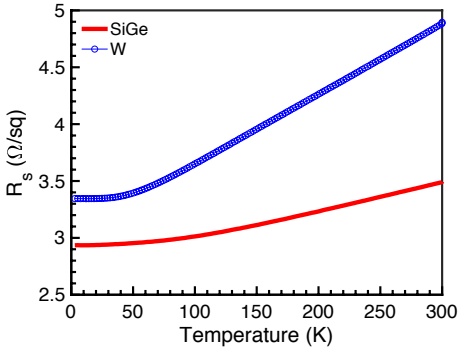


Fig. 11. Measured dependence of sheet resistance for the W electrode layer and poly-SiGe structural layer. *In-situ*-boron-doped poly SiGe does not show freeze-out effects and W also remains electrically conductive at temperatures as low as 1.8 K, indicating that MEM relays should function properly at 1.8 K.

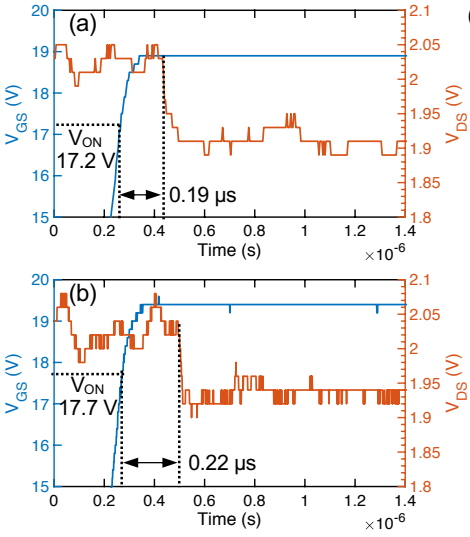


Fig. 12. Relay turn-on delay measurements with V_B = 0 V (a) at 300 K, (b) at 4 K.

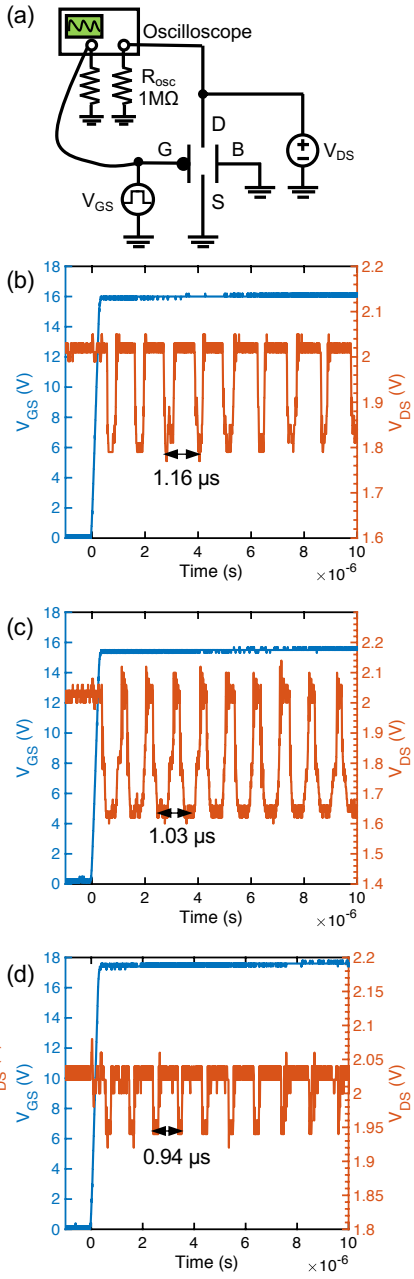


Fig. 8. Relay oscillator testing: (a) circuit schematic diagram; the measurement is performed at (b) 300 K, (c) 77 K, and (d) 4 K. From the measured average oscillation periods the natural frequency of the relay is 0.86 MHz at 300 K, 0.97 MHz at 77 K, and 1.065 MHz at 4 K, indicating that the structural stiffness increases with decreasing temperature.