Abstract—Non-volatile (NV) nano-electro-mechanical (NEM) switches are successfully implemented using multiple metallic layers in a standard 65 nm CMOS back-end-of-line (BEOL) process with no additional lithography steps. Non-volatile operation of a NEM switch as a reconfigurable interconnect to dynamically change CMOS circuit functionality is demonstrated.

Index Terms—Non-volatile switch, reconfigurable computing, monolithic integration, BEOL, interconnects.

I. INTRODUCTION

The emergence of the Internet of Things (IoT) has motivated research to develop more compact and energy-efficient integrated circuit (IC) chip products. Nano-electro-mechanical (NEM) switches have gained attention as an alternative to conventional transistors due to their lower energy consumption, non-volatile (NV) switching capability and abrupt switching characteristics that provide for a very large resistance ratio between programmed states [1]–[8]. Of greater potential impact, NEM devices used in conjunction with CMOS circuitry can provide for enhanced chip functionality and/or energy efficiency at relatively low incremental cost [9]–[15]. Specifically, the back-end-of-line (BEOL) metallic layers used to form interconnects in a conventional CMOS process can be leveraged to implement compact NV-NEM switches for dynamically reconfigurable circuit functionality [6], [16]–[22].

Recently, reconfigurable logic (RL) circuits implemented with electrostatically actuated interconnects were experimentally demonstrated using a conventional CMOS process and CMOS-compatible switching voltages [21]. In this paper, the following key improvements over the prior work are presented: the reconfigurable interconnects are implemented using NV-NEM switches with many BEOL layers, which is advantageous for achieving lower programming voltage and/or more compact layout and for greater design flexibility and switch functionality. Additionally, non-volatile operation with consistently low contact resistance is demonstrated.

II. RECONFIGURABLE INTERCONNECT DESIGN

Fig. 1 illustrates the schematic cross-section of a typical 65 nm CMOS metallization stack showing all the BEOL interconnect layers. The minimum metal pitch (MMP) is available for the lowermost layers of the stack, and the pitch becomes increasingly relaxed towards the top of the stack. The tight-pitch metallic layers at the bottom of the BEOL stack are advantageous for forming small actuation gaps for NEM structures, to achieve smaller operating voltage and/or a more compact footprint. In this work, NV-NEM switches are formed utilizing the bottom five metal layers of the BEOL stack, while the metallic layers above are used for electrically connecting the switch to probe pads and for masking the release etch process. This design approach differs from that used in previous works in which the top BEOL layer was used to form the actuation electrodes [19]–[21].

Fig. 2 shows scanning electron micrograph (SEM) images of an NV-NEM switch as a reconfigurable interconnect, fabricated using a standard 65 nm CMOS process. It has five terminals, labeled in Fig. 2(a): a movable beam, two programming electrodes (Program 0/1), and via layers, inter-metal dielectric (IMD) and intra-layer dielectric (ILD) layers.

Fig. 1. Schematic cross-section illustrating BEOL metallic interconnect layers in a standard CMOS process, including metal and via layers, inter-metal dielectric (IMD) and intra-layer dielectric (ILD) layers.
movable beam, and two corresponding contact electrodes (D0/1). Note that this NEM switch can function as a 2-to-1 multiplexer/demultiplexer, to route a signal applied to the beam through to either D0 or D1 terminal.

The beam, program and contact electrodes are constructed using five metal layers and intermediary via layers at the bottom of the BEOL stack, as shown in the cross-sectional SEM images in Fig. 2(b) and (c).

After completing the standard CMOS and BEOL fabrication process, the dielectric stack around the movable beam was etched in order to allow it to be actuated. Fluorine-based plasma was used for this high-aspect-ratio blanket etch which is fully compatible with standard BEOL materials. Using dummy patterns in the top metal layers as an etch mask, CF4-CHF3-He plasma was used for highly anisotropic etching and SF6-O2 plasma was used to provide the necessary undercut to release the movable beam. The etch process was controlled to cause minimum damage to the TiN/TaN liner material. As-fabricated, the movable beam is in the neutral position, neither contacting the D0 electrode nor the D1 electrode.

When a voltage of sufficient magnitude and duration is applied to either of the programming electrodes, the resultant electrostatic force causes the beam to actuate into contact with the corresponding contact electrode, as shown in Fig. 2(d). For example, this reconfigurable interconnect can be programmed into state “0” (with the beam contacting the D0 electrode) by applying a voltage pulse to the Program 0 electrode. In the programmed state, adhesive force exists between the beam and the contact electrode, which causes the beam to remain in contact even after the voltage applied to the programming electrode drops to zero, i.e., the state is non-volatile. To change the programmed state of the interconnect from state “0” to state “1”, a voltage pulse must be applied to the Program 1 electrode.

III. DEVICE CHARACTERISTICS

For non-volatile operation, the spring restoring force of the movable beam, \( F_k \), must be lower than the contact adhesive force between the beam and contact electrode, \( F_{adh} \), i.e.,

\[
F_{adh} > F_k.
\] (1)

The beam width and the contact area can be designed to tune \( F_k \) and \( F_{adh} \), respectively, to meet this requirement. The non-volatility of programmed state “1” is evident from the measured current-vs.-voltage characteristics shown in Fig. 3(a), for which the programming voltage, \( V_{prog} \), was swept up and down with 1.2 V and 0 V applied to the D1 and the beam, respectively. Change of state from “0” to “1” (write operation) occurs when \( V_{prog} \) exceeds the switching voltage at 9.75 V. During the programming cycles, the current through Program 0/1 is monitored to be less than 10 pA, which demonstrates that there is no physical contact (catastrophic pull-in) between the beam and the program electrodes. The non-volatile programmed states can be easily distinguished or read by applying 1.2 V between the beam and the D0 or D1 contacting electrode, which is compatible with the core \( V_{DD} \) of 65 nm CMOS. As the BEOL metal pitch is scaled down with continued advancement of CMOS process technology, operation of reconfigurable interconnects can become faster and more energy-efficient. Fig. 3(b) shows the simulated write voltage i.e. minimum \( V_{prog0} \) or \( V_{prog1} \) required to switch states for different technology nodes. The programming voltage, which scales down rapidly with MMP, is projected to be within the range compatible with input/output (I/O) circuitry for CMOS technology nodes at 22 nm and beyond.

In this work, the contact material is electroplated copper coated with liner material. Fig. 4 shows the measured reconfigurable interconnect contact resistance, \( R_{cont} \) obtained for different contact areas. These values represent a significant improvement to previous work using similar contact materials [20]. The lower contact resistance in this work can be
The NEM interconnect can be programmed to route the input signal, \( V_{IN} \) through the movable beam to either D0 or D1. D0 is connected to \( V_{OUT} \) directly, whereas D1 is routed to \( V_{OUT} \) through a CMOS inverter. \( V_{IN} \) is chosen to be a 100 kHz square wave signal swinging between 0 V and \( V_{DD} \). The NEM interconnect is chosen to have a relatively low contact resistance of a few hundreds of ohms.

With the interconnect programmed to the “0” state, \( V_{IN} \) is transferred to \( V_{OUT} \), as seen in Fig. 5(b), where the signal propagation delay is measured to be < 100 ns. (This \textit{read} delay is dominated by the large parasitic capacitances associated with the probe pads. It is to be noted that \textit{programming} or \textit{write} delay, which is larger than \textit{read} delay, is dominated by the mechanical movement of the beam.) As seen in Fig. 5(c), \( V_{IN} \) and \( V_{OUT} \) are complementary signals, when the interconnect is programmed to the “1” state, which demonstrates the functionality of the CMOS inverter fabricated underneath the BEOL layers. The large \( RC \) delay in \( V_{OUT} \) is due to the relatively high on-state resistances and parasitic capacitances of the CMOS transistors, exacerbated by the aforementioned large parasitic capacitances. This was verified by characterizing the standalone CMOS inverters without the presence of the NEM reconfigurable interconnect.

V. CONCLUSION

Non-volatile NEM switches as reconfigurable interconnects have been successfully implemented using multiple metallic layers in the BEOL stack of a standard 65 nm CMOS process. With technology scaling, the programming voltage of BEOL NV-NEM switches is projected to be in the range compatible with standard I/O CMOS circuitry. Operation of a hybrid CMOS-NEM circuit is demonstrated, verifying low contact resistance and reconfigurable circuit functionality, showing promise for future Internet of Things applications.

ACKNOWLEDGMENT

The CMOS chips were fabricated at Texas Instruments and post-processed in the UC Berkeley Marvell Nanofabrication Laboratory. The authors would like to thank Dr. R. Mih for useful discussions.

REFERENCES
