An Optically Sampled ADC in 3D Integrated Silicon-Photonics/65nm CMOS

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Abstract

The accuracy of conventional ADCs for high-frequency input signals is mainly limited by the sampling clock jitter. To address this issue, this paper demonstrates an ADC that uses low-jitter (<26 fs_{rms}) optical pulses to sample the input signal. A prototype two-channel ADC is realized in a 3D integrated platform with 65 nm CMOS and silicon-photonics connected using high-density TOVs. With optical pulses spaced at 250 ps (4 GS/s effective sampling rate), the ADC achieves SNDR of 40 dB near DC and 37 dB at 45 GHz input.

Introduction

As the silicon-photonics (SiPh) processes mature, high-performance optical blocks integrated close to CMOS can be leveraged to alleviate system-level performance bottlenecks. For instance, to achieve 6 bits of resolution at 45 GHz input, an ADC needs a sampling clock with <32 fs jitter. While this level of clock purity is unachievable for electrical oscillators, it is readily available with optical pulses derived from a mode-locked laser (MLL) [1]. Hence, sampling in the optical domain can improve ADC resolution at high input frequencies. Previous optically sampled ADCs (O-ADC) are either discrete [1, 2] or have low resolution [3]. This paper presents the first SiPh O-ADC fully integrated on a single-chip. The O-ADC is fabricated in a 300mm CMOS foundry and achieves >5.5-bit resolution and input sampling bandwidth of 45 GHz.

Architecture of an Optically Sampled ADC (O-ADC)

Figure 1 shows the architecture of an O-ADC. An MLL-based external optical pulse source generates pulses at wavelengths λ_1 to λ_N with a pulse width τ, spacing t_S, and a repetition rate T_{rep}. An electro-optic modulator modulates the intensity of these pulses with the input signal. These pulses are then coupled into a SiPh chip where they are separated by the tunable double-ring bandpass filters that are matched to λ_1–λ_N. Here, a two-channel (N=2) O-ADC with (λ_1=1548.5nm) and (λ_2=1550.12nm) is demonstrated. Thermal tuning circuits on the CMOS chip tune the filters to the desired wavelength. Photodetectors in each channel convert the optical pulses into current pulses that are amplified and digitized by the analog frontend (AFE) on the CMOS chip. The AFE in Fig. 2 comprises an integrator, pre-amplifier, and an 8b asynchronous SAR. During Φ_1, the detector current is integrated for T_{Int} duration on the sampling capacitors C_{S1} and C_{S2}. As the optical pulses have a fixed width, the integrator acts as an amplifier with gain $\tau/2C_S$. The benefits of using an integrator are that it eliminates the adjacent channel cross-talk current pulses occurring after a time interval of t_S, limits the effect of detector's shot noise, and suppresses the impact of CMOS clock jitter (for $T_{Int} >> \tau$). During Φ_2, the single-ended voltage across $C_{S1,2}$ is converted to differential by transferring the charge from C_{S1} and C_{S2} to C_F by switching the bottom and the top plates, respectively. Also, during Φ_2, the SAR ADC samples the voltage on the top plate of the 7b capacitive DAC. Once the input is sampled, the asynchronous SAR logic generates the necessary control signals and comparator clock Φ_C until all 8 bits are resolved. The SAR ADC's measured DNL/INL are within ±1 LSB at 500 MS/s.

Wafer-scale 3D Integrated Silicon-Photonics/65nm CMOS

The O-ADC is realized in a wafer-level 3D heterogeneous integration platform shown in Fig. 3. The circuits are designed in 65nm bulk CMOS LP-process, while the SiPh devices are fabricated on a 300mm SOI wafer with 220nm Si thickness and 2µm buried oxide using 193nm immersion lithography. The SiPh wafer is flipped and direct oxide bonded with the CMOS wafer. To avoid defects at the bond interface, the wafers' surfaces are smoothed down to 0.5nm_{rms} roughness. The copper through-oxide vias (TOVs) are drilled with a pitch of 7µm to connect the SiPh devices to the CMOS circuits, and wirebond pads and device connections are formed using the backmetal. Figure 3 shows the geometry and the cross-section of double-ring filters and the detector. At resonance, a double-ring filter couples optical power from the bus waveguide to the detector on its drop-port. The filters are designed to resonate at λ_1 and λ_2, and have a wide free spectral range of 34nm [4]. A vertical *p-i-n* junction Ge-on-Si detector with a responsivity of 0.9 A/W, 30 GHz bandwidth, and <10nA dark current is used.

O-ADC Demonstration

Figure 4 shows a photo of the finished wafer and the test chip. To test it, an MLL-based optical pulse source is used with T_{rep} of 100MHz, jitter of 26 fs_{rms}, τ of 3 ps, and t_s of 250 ps. As this source outputs only two 250 ps spaced pulses per T_{rep}, an equivalent time signal is constructed by accumulating multiple samples. An off-chip 40 GHz bandwidth MZM modulates the optical pulses. Before the input is sampled, the offset, pre-amplifier gain mismatch, and gain error due to mismatches in the detector's responsivity and filters' drop-port spectrum (Fig. 5b) are calibrated in the foreground. Thermal tuners in Fig. 5a compensate for process and thermal-induced shift in filter resonance up to 2.5 nm with 9 µW/GHz efficiency. Also, to minimize the filter's distortion (Fig. 5c), the incident optical power is limited to 8 mW (10-bit shot-noise limited resolution). The MZM's static non-linearity is corrected from the O-ADC output [1]. Figure 6 shows the FFT for a 1.85 GHz input. The cross-talk is induced intentionally by making $T_{Int} = 2t_s$. With calibration applied and using the right $T_{Int} = t_s$, the SNDR improves by 5.5 dB. The FFT for 44.73GHz input shows an SNDR of 36.9 dB mainly limited by modulator's HD3, and the SNR of 40 dB provides an upper bound on sampling jitter of 36 fs [7]. Figure 7 shows the SNDR and SFDR over an input range of 2 MHz to 45 GHz. Table-I compares this work with the prior art. This design is the first demonstration of a fully integrated optically sampled ADC fabricated in a CMOS foundry. Compared to the state-of-the-art CMOS ADCs, it achieves the highest SNDR for >40GHz input and a sampling bandwidth of 45 GHz, widest reported.

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References

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[5] L. Kull et al., VLSI Symp 2018. [6] Y. Greshishchev et al., ISSCC 2010.

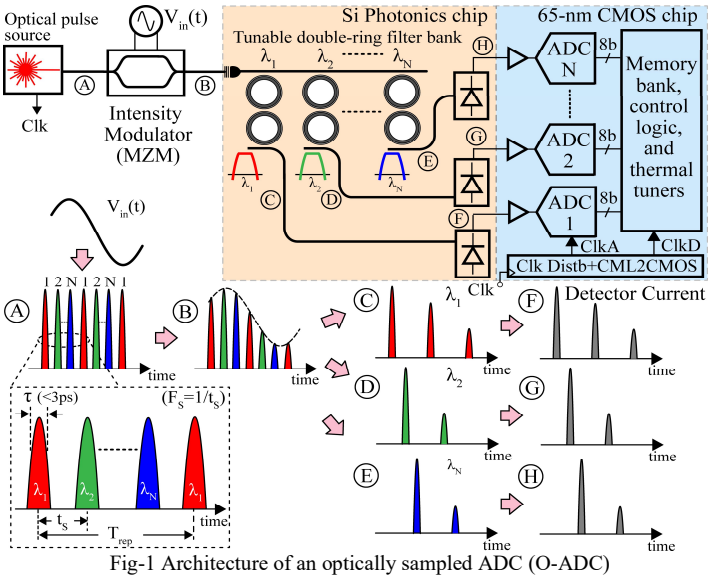


Fig-1 Architecture of an optically sampled ADC (O-ADC)

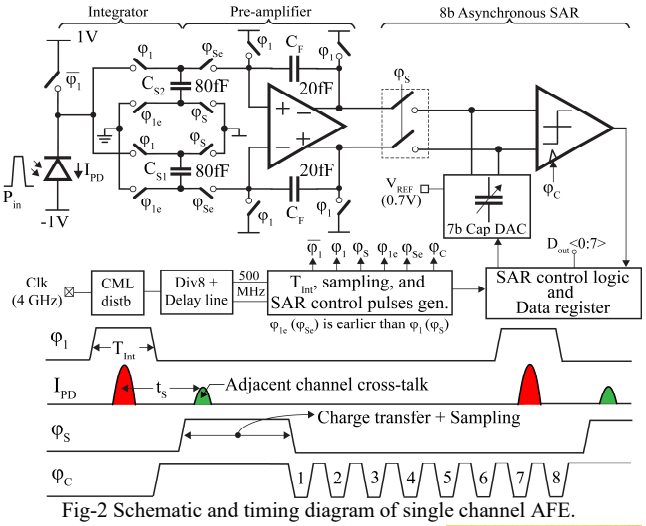
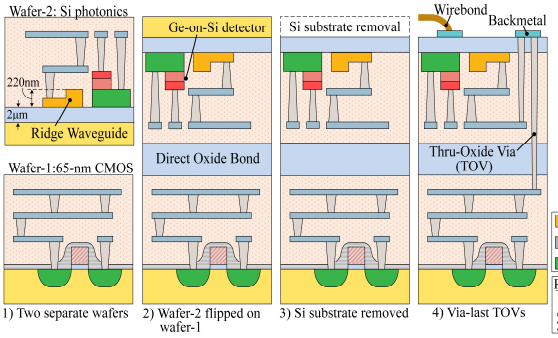


Fig-2 Schematic and timing diagram of single channel AFE.



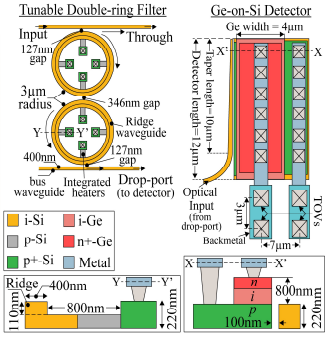


Fig-3 Wafer-scale 3D integration of SiPh/CMOS. Structure of double-ring filter and the detector.

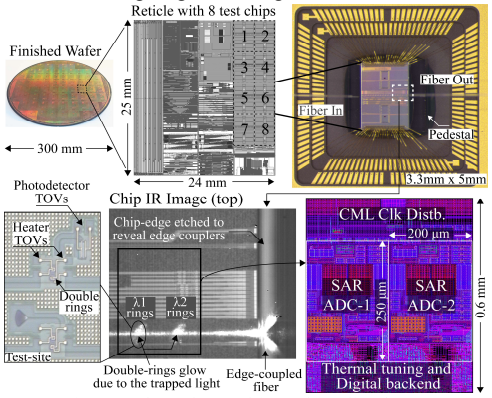


Fig-4 Packaged test-chip and its die photo.

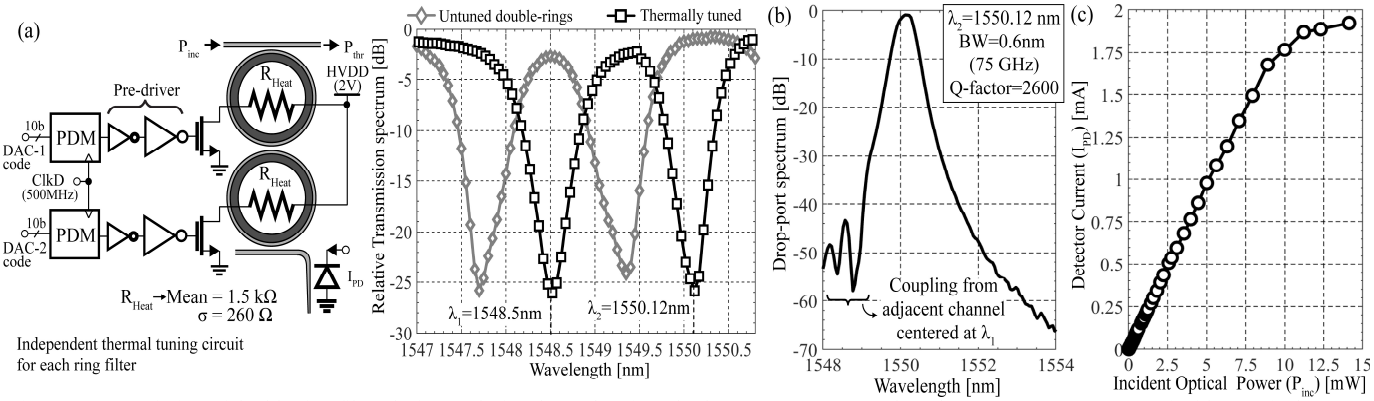


Fig-5 (a) Transmission of double-ring filters before and after thermal tuning, (b) drop-port spectrum and (c) detector current vs average incident optical power.

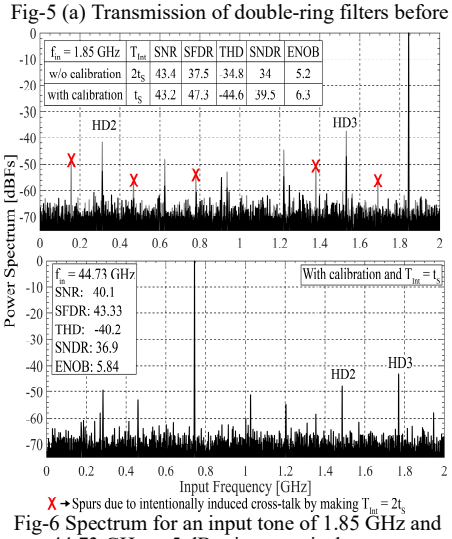


Fig-6 Spectrum for an input tone of 1.85 GHz and 44.73 GHz at 5 dBm input optical power.

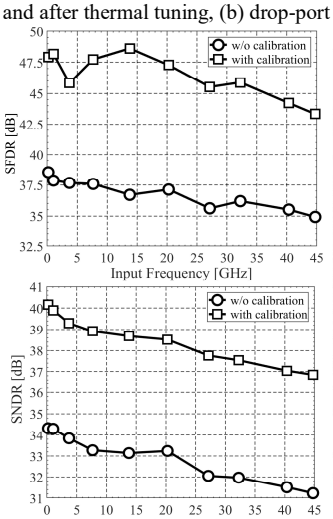


Fig-7 SFDR/SNDR vs. input freq.

Table-1 Performance summary and comparison with prior works

	This Work	[3] JSSC'03	[2] CLEO'11	[5] VLSI'18	[6] ISSCC'10
Sampling Architecture	Optical pulse based			Electrical	
Technology	**3D Integrated Si-Ph w/65nm**	250nm CMOS w/ LT GaAs	Discrete off the shelf	14nm FinFET CMOS	65 nm CMOS
Supply Voltage [V]	**1.2/1.5/2**	2.5	2/5†	0.8/0.95*	1/1.2/2.5
Resolution [bits]	**8**	4	9	10	6
Sampling Rate [GS/s]	**4**	0.16	2	32	40
SNDR near DC [dB]	**40.2**	24†	–	47.3	34.9
$f_{in,high}$ [GHz]	**44.73**	40	40	39.8	18
SNDR at $f_{in,high}$ [dB]	**36.9**	23.4	43.8	37.8	25.2
Power [mW]	**88**#	140#	–	199	1500
Area [mm²]	**0.25**‡	0.068	–	0.16	16

*SAR ADCs/Interleaver+Sampler. †Estimated from given data. ‡Includes optical blocks. #Electrical power only

Power breakdown of the complete O-ADC system					
	Supply [V]	Power [mW]		Supply [V]	Power [mW]
AFE (integrator+Amplifier) (x2)	1.5	42.2	CML Clk-distb+delay lines	1.5	5.8
Async SAR @ 500MS/s (x2)	1.5	24	Heater Driver (x4)	2.0	3
Thermal tuning logic @ 500MHz (x4)	1.2	3.2	Memory bank + control logic	1.2	9.8
Optical power required by O-ADC		7	Optical pulse source power		4000