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A Single-Chip Optical Phased Array in a Wafer-Scale Silicon Photonics / CMOS 3D-Integration Platform

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***Abstract*— With the growing demand for automotive LiDAR and the maturation of silicon photonics platforms, optical phased arrays (OPAs) have emerged as a key technology for solid-state optical beam-steering. In order to meet realistic automotive specifications with OPAs, >500 antenna elements should work reliably under tight power and cost budgets. Existing multi-chip solutions necessitate expensive packaging and assembly to achieve high interconnect density. Even with 2-D monolithic integration, high-voltage drivers to deliver sufficient power to resistive phase shifters typically result in significant overhead in die area and limited power efficiency. In this article, we introduce a single-chip OPA realized through wafer-scale 3-D integration of silicon photonics and CMOS. Flexible and ultra-dense connections with through-oxide vias (TOVs) in our platform resolve the I/O density issue. Moreover, low-voltage L-shaped phase shifters and compact, efficient switch-mode drivers, connected vertically using TOVs, remove wiring/placement overhead and achieve a large active array aperture within a compact die. Our OPA prototype achieves wide-range 2-D steering over 18.5° × 16° by leveraging wavelength tuning and phase control, and array scaling up to 125 elements with a large aperture size of 0.5 mm × 0.5 mm and 0.15° × 0.25° beamwidth while consuming 20 mW/element average power. Since our system supports per-element independent phase control, increased sensitivity to process variations in L-shaped shifters is fully compensated by a simple calibration process.**

***Index Terms*— 3-D integration, LiDAR, optical phased array (OPA), silicon photonics, solid-state optical beam-steering.**

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I. Introduction

OPTICAL beam formation and scanning techniques are currently in high demand, largely due to the rising need for LiDAR systems. LiDAR can offer better diffraction-limited lateral resolution compared to RADAR because its wavelength is >1000× smaller. As a result, it is widely considered to be a key sensing modality for the realization of reliable autonomous systems, most notably for self-driving cars [1]. At the same time, these emerging applications impose new challenges to LiDAR system design. For instance, automotive LiDAR demands outdoor operation with long detection ranges (>100 m), which is an extremely challenging requirement for traditional time-of-flight (TOF) cameras with flash illumination. To compensate for the significant signal-to-noise ratio (SNR) degradation in these scenarios, it is often critical to focus the laser power within a single pixel by forming a beam and scanning it to cover the whole field of view (FOV). Beyond LiDAR, high spatial resolution of the optical beams can also enable fast and secure wireless communication [2] and can even potentially serve as the next-generation propulsion mechanism for spacecraft [3].

Beam scanning modules in existing commercial products are largely based on mechanical control, such as motor-driven rotating collimation stages/mirrors [4] or galvanometers. In order to make those high-precision mechanical systems work reliably in an unstable environment (e.g., cars), they typically include a number of moving parts and tend to be bulky and slow, which is undesirable as it also leads to large size, increased weight, and high power consumption. More importantly, they require a complex assembly and calibration process, which results in extremely high unit cost. Largely due to this cost issue, LiDAR is currently not considered for use in mass production vehicles. This has motivated active research on optical beam-steering techniques that minimize mechanical movements or are completely solid-state during operation. Existing techniques include micro-electromechanical systems (MEMS) mirrors [5], lens-assisted emitter arrays [6], [7], liquid crystal waveguides [8], and photonic crystal waveguides combined with diffraction gratings [9].

Optical phased arrays (OPA) are one of the most promising solutions for solid-state beam-steering. Radio frequency/mm-wave phased arrays are already prevalent in

RADAR and wireless communications, and it is also possible to realize the same concept in the optical domain. This technique has gained a lot of attention alongside advancements in silicon photonics technology, which enables inexpensive fabrication of a large number of optical components [10], [11]. OPA technology has progressed tremendously within a relatively short period of time, and multiple large-scale implementations with ∼1000 elements recently reported [12]–[16].

However, it is still challenging to realize a low-cost OPA that can bring the proliferation of chip-scale optical beam scanners to mass markets. For instance, to meet the resolution and field-of-view requirements for automotive LiDARs, the element count should reach 500–1000. The majority of prior OPA demonstrations take a multi-chip approach where photonics and electronics are present on separate chips, and the number and density of I/O connections and electronic circuits clearly exceed the limits of low-cost packaging options. Several OPA architectures have been proposed to reduce the number of independent electrical signals [15]–[17] by trading off the array control flexibility.

Ultimately, a single-chip solution is desired to completely resolve the I/O and electronics density problem at a minimum unit cost with guaranteed performance in the presence of process- and design-dependent phase uncertainty. 2-D monolithic integration of electronics and photonics in an SOI process is one technique of realizing a single-chipOPA [15], [18]. However, physical constraints due to CMOS design rules and limited material/processing steps significantly constrain photonics design and make it hard to meet system requirements. Moreover, thermooptic phase shifters, often used in such OPAs, consume a significant amount of maximum power and require high voltage swings. Delivering large amount of power through each of the 1000s of on-chip interconnects tends to cause routing/placement congestion, large die size, and significant circuit power overhead due to limited driver efficiency and voltage droop.

In this article, we realize a single-chip OPA on a wafer-scale 3-D integration platform, which allows for photonics and CMOS electronics to be independently optimized while enabling flexible, dense vertical connections between them [19]. We introduce key OPA building blocks that leverage the uniqueness of our platform, including apodized grating antennas that maximize the array effective aperture and low-voltage L-shaped thermooptic CMOS-compatible phase shifters, connected vertically to pitch-matched pulse density modulated (PDM) switch-mode drivers, completely eliminating the placement/wiring overhead and achieving an area- and power-efficient system suited for large-scale OPAs. We experimentally validate our OPA architecture with a successful demonstration of 2-D wide-range beam-steering and with a large array aperture. We also demonstrate full-array calibration with per-element phase control, which resolves static passive beam pattern distortion.

The remainder of this article is organized as follows. Section II introduces requirements for OPA in the context of automotive LiDAR and presents an overview of practical challenges associated with meeting the desired performance. Section III introduces the wafer-scale 3-D photonics–electronics heterogeneous integration platform used for our single-chip OPA. Section IV provides the overview of our OPA architecture as well as building block design considerations. Then, the experimental demonstration of our single-chip OPA is presented in Section V. Section VI revisits the system requirements to discuss the remaining challenges and illustrates future directions. Finally, Section VII concludes this article.

II. Optical Phased Arrays for Robust High-Resolution Beam Scanning

A. OPA LiDAR System Requirements

To get a sense of what the performance expectations are for OPAs from a system-level perspective, we can refer to the beam scanner specifications shared across the automotive industry. The main performance metrics and their respective values [20], [21] are as follows.

1) *Lateral Resolution:* 0.1°–0.2° (horizontal and vertical).
2) *FOV:* >90° (horizontal).
3) *Power Budget:* 10–30 W.
4) *System Cost:* $100–$200.

Above all, the scanner must satisfy the resolution requirements so as to recognize small objects (e.g., pedestrians) at a long distance. The relationship between the array parameters and the beam resolution [or full-width at half-maximum (FWHM)] is well known [22]

$$\mathrm{FWHM} = \cos^{-1}\left(\sin\theta_{\mathrm{b}} - \frac{2.78\lambda}{2\pi Nd}\right) - \cos^{-1}\left(\sin\theta_{\mathrm{b}} + \frac{2.78\lambda}{2\pi Nd}\right) \tag{1}$$

where θ_{b} is the beam angle (0 for upright), d is the antenna spacing, N is the antenna count, and λ is the wavelength, respectively. For a given wavelength, one can note that the lateral resolution is determined solely by the absolute size of the total aperture ($W = Nd$). For example, 0.2° worst case resolution for 90° FOV and $\lambda = 1550$ nm requires $W = 0.54$ mm.

Meanwhile, the ambiguity-free steering range of a phased array is determined by the antenna spacing

$$\mathrm{FOV} = 2\sin^{-1}\left(\frac{\lambda}{2D}\right). \tag{2}$$

For example, the spacing should decrease until it meets the range requirement, which results in increased number of antennas. For instance, 90° FOV would require 0.71λ-spacing ($d \sim 1.1$ μm), which corresponds to 490 antennas for $W = 0.54$ mm. Alternatively, one can achieve the same FOV with two adjacent OPA channels and relax the spacing to 1.3λ ($d \sim 2$ μm). The total number of elements is then $2N = 2(W/d) = 540$, slightly higher than the single-channel case. This level of OPA multiplexing would eventually be limited by power and cost constraints. Note that this pitch-FOV trade-off can potentially be relaxed through non-uniform antenna placement [13], [16], which alters the basic relationship of (2). Nevertheless, to be a compelling alternative to mechanical beam scanners, a clear path to scale the element count to 500–1000 is a must.

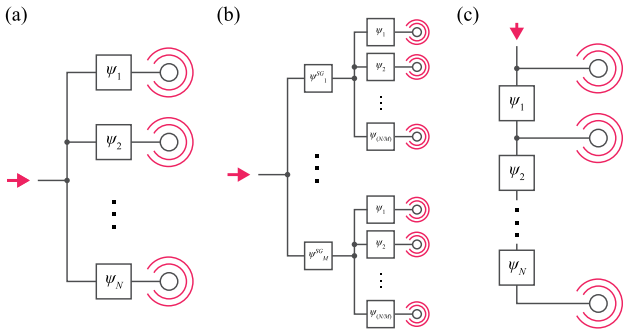


Fig. 1. OPA distribution network types (a) tree architecture, (b) grouped tree architecture, and (c) cascaded architecture.

B. OPA Architectures and Reduced Interface Complexity

In typical OPA implementations, to ensure coherence across the overall array aperture, a single laser source is used and evenly distributed to feed the antenna elements. Given this, the most simple and straightforward OPA architecture is the tree architecture [Fig. 1(a)], where a 1:N optical power splitter distributes the input power into N waveguides each connected to its own phase shifter and an optical antenna. Since the tree architecture mandates N independent phase shifters to address all possible beam directions within the FOV, the I/O and electronics density associated with 500–1000 antenna elements have made it challenging to realize a low-cost OPA for practical applications, especially based on a multi-chip integration strategy where photonic and electronic circuits are realized in separate chips and packaged on a cheap substrate.

This has motivated various works to propose alternative OPA architectures that reduce interface/control complexity. One possible option is to change the optical distribution network architecture to a grouped tree structure [Fig. 1(b)] [15]. In this design, antennas and associated phase shifters are divided into M subgroups, and each subgroup has its dedicated phase shifter at its root of the splitter tree to adjust the phase offset between subgroups. For a linear phase ramp, a single set of signals can be shared over the whole array to control the phase shifters within each subgroup. As a result, the overall independent signal count in grouped tree architecture is $M + N/M$. The level of subgroup hierarchy can also be further increased [15] to improve the granularity of the phase adjustments.

Another solution is the cascaded architecture [Fig. 1(c)] [17]. In this design, optical power distribution is done through a series of couplers placed along the bus waveguide, and the phase shifters are located between those couplers. For example, the phase shifter adjusts the relative phase difference, rather than the absolute phase. For a phase ramp required to perform linear scanning, the relative phase between adjacent shifters is always constant across the array. As a result, only one control signal is enough to support all beam positions. Similar to the grouped tree, this architecture can also be segmented (i.e., grouped cascade) and driven by multiple signals to introduce additional flexibility to the phase pattern [17].

Finally, it is worth noting that instead of modifying the optical distribution network, it is also possible to utilize the slow transient response of thermooptic phase shifters to reduce the interface complexity. In [16], phase shifters are placed in a rectangular array, and the phase shifters within one row are addressed individually through a single row wire in a time-shared fashion using pulsewidth modulated (PWM) signal. By synchronizing row PWM signals to the activation signal on the column wire, only 37 wires were used to address 128 phase shifters in [16].

C. Process and Design-Dependent Random Phase Fluctuation

One of the well-known issues in silicon photonics that could limit the use of OPAs in mass markets is waveguide coherence [23]. Process variation-induced nanoscale uncertainties in waveguide geometry perturb the effective index and result in random fluctuations of phase [24], disrupting spatial coherence at the array aperture. Still, phase perturbation from process variation is a static error and can be corrected through proper calibration processes. In [15], it was concluded that assuming reported levels of variation for standard strip waveguides fabricated in an SOI process [24], it is possible to maintain decent OPA performance with a grouped tree architecture of subgroup size $N/M = 8$ by adjusting phase offset between subgroups.

However, it must be noted that the waveguide coherence is heavily dependent on the actual fabrication process as well as the geometry of the designed components. This is especially the case in thermal phase shifters where the temperature dependence of the silicon index is utilized to adjust the phase. As noted in Section II-A, the total power budget of the LiDAR system is only on the order of 10s of watts, and it is important to optimize the efficiency of the heater and driver circuits to support large element count. A popular way to enhance the heater phase efficiency is directly embedding the resistive segment of the heater into the waveguide so that the thermal impedance between the heater and the waveguide core is minimized [25]. At the same time, in order to reduce the heater driver circuit complexity, the heater resistance should be decreased to bring the voltage swing down to CMOS-compatible levels, which requires high heater contact density.

As explained later in detail (Section IV-B), we have designed a thermooptic phase shifter with an L-shaped waveguide where the heater is embedded into a one-sided slab layer to achieve high efficiency and low resistance. However, slab waveguides are known to have much worse waveguide coherence due to additional error sources, including a partial etch step [24]. For example, an analysis based on the coherence of simple strip waveguides can be rather optimistic, especially in OPAs where components are heavily optimized to satisfy the power and area constraints. As explained in Section IV, this eventually motivated us to pursue per-element phase control flexibility, which completely desensitizes OPA performance to the level of device coherence.

III. Wafer-Scale 3-D Heterogeneous Integration of Silicon Photonics and CMOS Electronics

In [15] and [18], 2-D monolithic integration of photonics and electronics on a common SOI CMOS substrate was

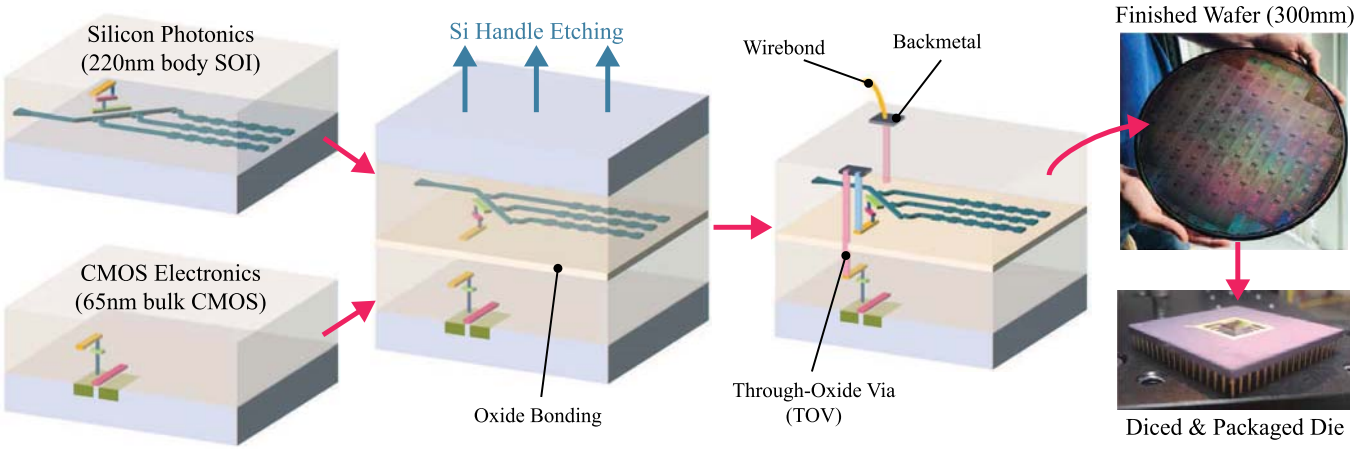


Fig. 2. Overview of the 3-D heterogeneous integration platform used to construct the single-chip OPA.

presented as a low-cost solution to I/O complexity issue, realizing a single-chip OPA and up to ∼1000 element count [15]. However, 2-D monolithic integration has a few critical disadvantages in the context of OPAs. First, a photonic device design is limited due to CMOS design rules and available materials and processing steps. Moreover, side-by-side placement of photonics and CMOS tends to cause placement/routing congestion in large-scale arrays. Typical thermal phase shifters consume up to 50–100 mW of power and require ∼10 V swing, which mandates wiring via thick top-layer metal to minimize the IR loss over the interconnect as well as stacked thick oxide devices, which makes it very challenging to realize compact driver circuits. As a result, OPAs in monolithic platforms often result in a large die footprint for small active array apertures [15], [18].

In this article, we realized single-chip OPAs on a 3-D heterogeneous integration platform shown in Fig. 2, similar to [26]. The integration process starts with two independently optimized 300 mm wafers. Photonic devices are fabricated with 193 nm immersion lithography on a SOI wafer with 220 nm body thickness (typical waveguide loss is 3 dB/cm for the 1500–1600 nm wavelength range), while electronics are implemented using a standard CMOS technology. A 65 nm low-power bulk CMOS process was used in this article, but in principle, any process can be used as long as it has the matching wafer size to the photonics as well as acceptable transistor and wiring density. The two wafers are then face-to-face oxide-bonded at the wafer scale, and the silicon handle on the photonic wafer is globally etched down to the buried oxide (BOX).

After the wafer bonding and etching, through-oxide vias (TOVs) are formed to establish the electrical connections between CMOS and photonics. TOVs can be densely placed at arbitrary locations with a pitch as small as 7 μm and have extremely low parasitic capacitance (∼3 fF), which can be treated just like top-level metal vias in the CMOS backend. Finally, the back-metal is placed for pads and TOV-pad connections.

The final result is a single 300 mm wafer, which can be further processed following the standard CMOS packaging steps, including dicing and wire-bonding to a ceramic package. Compared to the die-scale vertical integration often used for optical transceivers [27], much higher (>7×) interconnect density versus copper pillars, flexible via/circuit placement that minimizes wiring/placement overhead, and lower unit cost of wafer-scale 3-D integration make our platform better suited for OPAs.

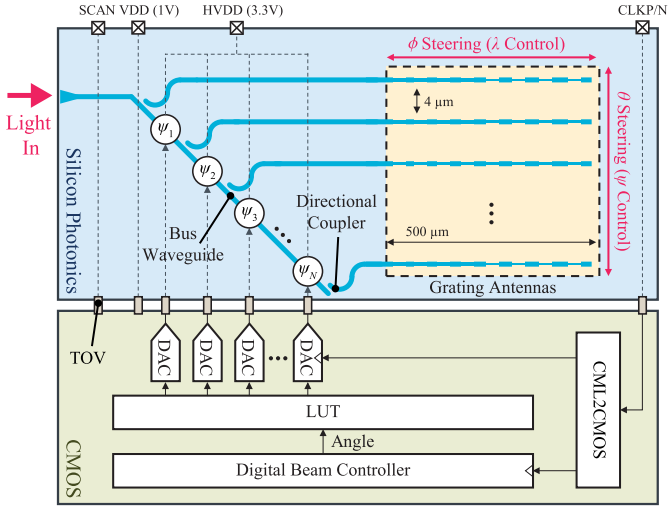


Fig. 3. Overview of the single-chip OPA architecture.

IV. Optical Phased Array Implementation

Fig. 3 shows an overview of the single-chip OPA prototype implemented on our 3-D integration platform. The design is based on a cascaded array architecture from Section II-B. The advantage of the cascaded architecture in our prototype was twofold. First, since it is possible to apply a nominal steering signal through a single wire, it is easier to examine the level of phase uncertainty before packaging using a simple probe. Second, the cascaded architecture is generally less affected by thermal crosstalk [28] since the nominal phase pattern does not have discontinuities coming from limited phase shifter range, unlike the (grouped) tree architecture. Nevertheless, any

architecture can eventually be supported once the functionality of the system is verified, and we will revisit this in Section VI.

The input laser is coupled into the on-chip bus waveguide from a lensed fiber via an edge coupler. Cascaded directional couplers placed along the bus waveguide distribute the light into each optical antenna element. Thermooptic phase shifters are embedded into the bus waveguide sections between the couplers to adjust the relative phase offset of the adjacent antenna elements. Ultimately, this enables beam-steering along the direction of the array placement (θ in Fig. 3). The elements are placed at a 4 μm pitch in our prototype, which corresponds to the theoretical steering range ($2|\theta_b|_{max}$) of 22.3° at λ = 1550 nm from (2). However, the antenna elements used in our article can be placed at a tighter pitch down to the wavelength scale without inter-antenna evanescent coupling [25]. Each thermal phase shifter is independently driven by a CMOS controller based on a switch-mode digital-to-analog converters (DACs). Such per-element independent control guarantees optimum OPA performance through calibration regardless of design- and process-dependent photonic component coherence. This also mitigates potentially compromised robustness in the cascaded architecture due to the fact that the failure in one phase shifter affects all subsequent antennas: impact of one broken shifter is limited by introducing phase bias to the following shifter. DAC inputs are provided by an on-chip lookup table (LUT) that has the beam position codes after array calibration, enabling rapid steering along arbitrary trajectories.

In addition, our antenna enables the main radiation direction of an individual element to be tunable by the laser wavelength. For example, the beam-steering along the direction orthogonal to the array placement (ϕ in Fig. 3) is done through wavelength tuning, achieving full 2-D beam-steering. The details of the antenna element, the thermooptic phase shifter, as well as the control circuit design are described in Sections IV-A–IV-C.

A. Apodized Grating Antenna

Fig. 4(a) shows our optical antenna concept. The antenna is a long 400-nm-wide waveguide grating formed by fully etched sidewall perturbations, where the perturbed waveguide section creates a local effective index mismatch. As a result, when the light propagates through this grating, a certain fraction of light is scattered into free space at every perturbed section. The overall length of our grating antenna is 500 μm, which enables a large emitting aperture and small divergence angle in ϕ (~0.15°). This is unlike previous work where short grating couplers (3.55 μm long) with divergence angles over 10° were used as emitting elements [15].

Note that the light scattering ratio due to the local index contrast is determined by the depth of sidewall etching. To produce a uniform emission profile and maximize the effective aperture of the antenna, the perturbation depth has to increase down the length of the antenna (i.e., the perturbation must be apodized [29]). At the same time, to maintain the same optical path offset between neighboring scattering points, the physical distance between perturbations (Δx) should also gradually increase. The 1 nm resolution of the photolithography masks

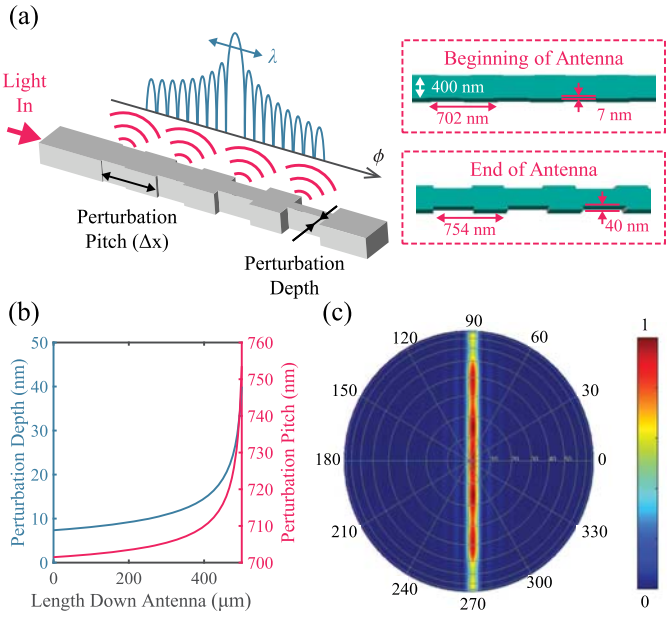


Fig. 4. (a) Apodized grating antenna overview and the dimensions at the beginning and at the end of the antenna. (b) Perturbation distance and pitch distribution across the antenna element. (c) Antenna emission pattern from an finite-difference time domain (FDTD) simulation.

used, allows for near infinitesimal changes in perturbation strength [Fig. 4(a) and (b)], again highlighting the benefit of utilizing fully customized photonics.

The reader may note that a grating antenna composed of repeated scattering points resembles a 1-D phased array. In this case, the relative phase difference between emitting elements is set by the optical path between scattering points. The following relationship can be established to determine the position of the main beam in ϕ:

$$\frac{2\pi}{\lambda}\Delta x(\sin\phi + n_{\text{eff}}) = 2\pi M, \quad M \in \mathbb{Z} \tag{3}$$

$$\phi_b = \sin^{-1}\left(\frac{M\lambda}{\Delta x} - n_{\text{eff}}\right) \tag{4}$$

where n_{eff} is the effective index of the silicon waveguide. We designed the grating to satisfy $n_{\text{eff}}\Delta x = \lambda$, $M = 1$ at λ = 1550 nm. Since ϕ_b depends always on λ, beam-steering along ϕ is possible via input wavelength tuning, where steering efficiency is expressed as follows (n_g: waveguide group index):

$$\frac{d\phi_b}{d\lambda} = \frac{\frac{1}{\Delta x} - \frac{dn_{\text{eff}}}{d\lambda}}{\sqrt{1-\left(\frac{\lambda}{\Delta x} - n_{\text{eff}}\right)^2}} = \frac{n_{\text{eff}}}{\lambda} + \frac{n_g - n_{\text{eff}}}{\lambda} = \frac{n_g}{\lambda}. \tag{5}$$

The simulated group index at λ = 1550 nm is 4.43, which results in a steering efficiency of 0.164° per 1 nm wavelength shift.

B. L-Shaped Thermooptic Phase Shifter

As introduced in Section II-C, we had two key objectives for phase shifter design: high phase efficiency and CMOS-compatible swing. Fig. 5 shows a perspective view of the layout details around the bus waveguide, the cross

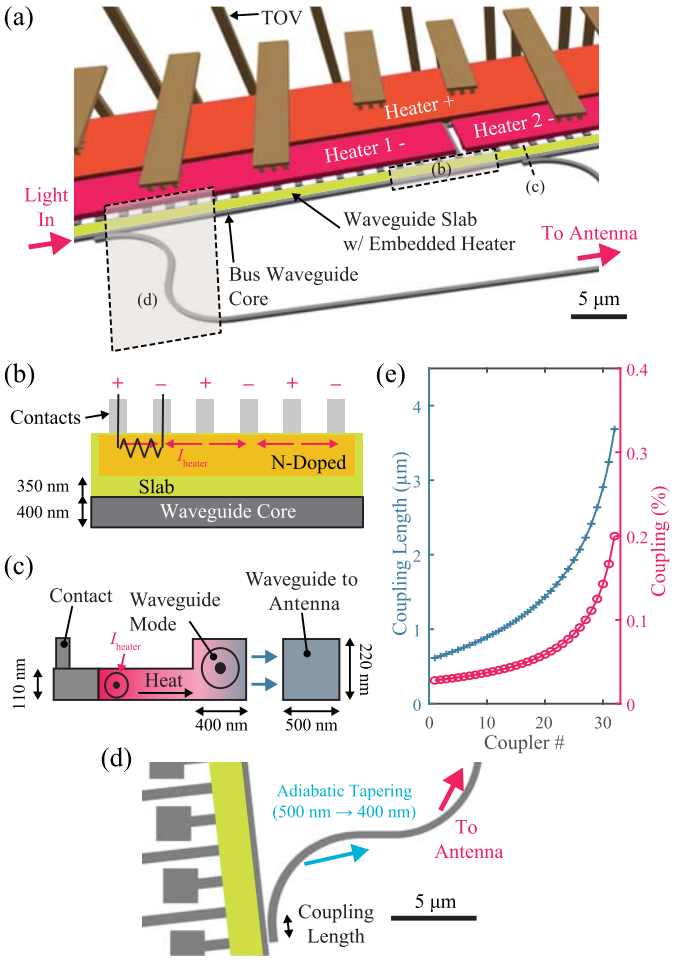


Fig. 5. (a) Perspective view of the layout details around the bus waveguide section including embedded thermooptic phase shifter and directional coupler. (b) Top view and (c) cross-sectional views of the L-shaped phase shifter. (d) Bus waveguide antenna connection through a directional coupler. (e) Evanescent coupling strength distribution across the bus waveguide for uniform power distribution.

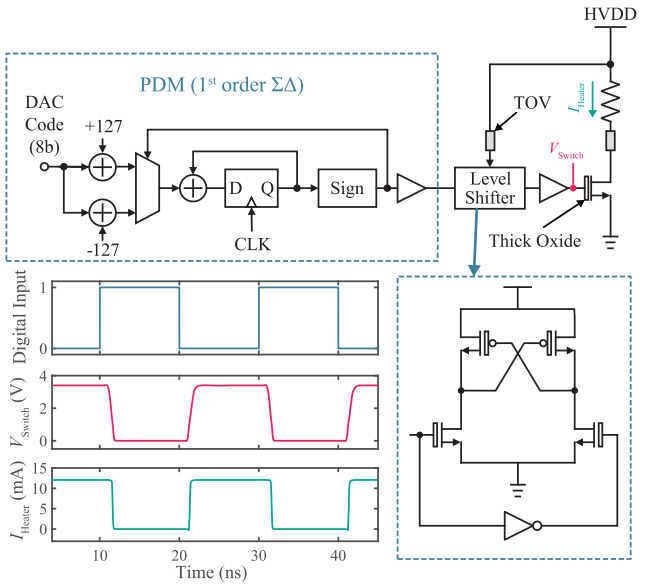


Fig. 6. Overview of the PDM-driven switch-mode driver connected the photonic heater element, as well as the simulated time-domain waveforms of PDM signal, heater switch gate voltage, and heater current.

section and top-view of the heater segment, and the layout of directional coupler connected to antenna elements. The bus waveguide is L-shaped, with a partially etched 110-nm-thick slab on one side of a 400-nm-wide 220-nm-thick core [Fig. 5(b) and (c)]. A resistive heater is directly embedded into the bus waveguide by N-doping the slab, 350 nm away from the waveguide core [Fig. 5(b)]. This ensures low thermal impedance between the heater and the core, resulting in high thermal efficiency (20 mW/π from COMSOL simulation). At the same time, the waveguide mode and doped region are isolated in the L-shape geometry [Fig. 5(c)], which ensures minimum optical loss (simulated loss: 0.016 dB). The length of one phase shifter is 32 µm, and considering that the thermooptic coefficient of silicon at 1550 nm is $1.8 \times 10^{-4}\,\mathrm{K}^{-1}$, 2π shift corresponds to 270 K temperature range.

N-doped slab layer also contains large clearance to form dense contact tethers and lower the resistance. In addition, multiple positive and negative contacts are formed in an interleaved fashion, resulting in an alternating current direction within the heater segment and resistors in parallel [Fig. 5(b)]. This ensures consistent current density (i.e., removal of hot spot and electromigration-limited segments) and low resistance. The resulting resistance of the phase shifter was 270 Ω, corresponding to 3.3 V voltage and 12.2 mA current swing.

Between the phase shifters on the bus waveguide, directional couplers are formed by placing strip waveguides on the other side of the bus waveguide core [Fig. 5(c) and (d)]. The strip waveguides have a width of 500 nm in order to achieve phase-matching to the L-shaped waveguide and efficient evanescent coupling (simulated loss: 0.015–0.02 dB across 1500 nm–1600 nm). The coupling strength of each directional coupler is gradually increased to ensure uniform distribution of the optical power across the entire aperture [Fig. 5(e)]. After the desired length of evanescent coupling, the strip waveguide is separated away from the bus ridge waveguide and adiabatically tapered back to a single-mode width of 400 nm for routing to the antenna.

C. Switch-Mode Heater Driver with PDM Modulator

During a beam scanning operation, each heater is expected to consume 20 mW of power (π shift in average across the FOV), which amounts to 10 W for a 500-element OPA. This is already comparable to the total power budget for the entire LiDAR system (Section II-A), which leaves no room for CMOS power. Therefore, it is imperative to ensure that the electrical power consumed in the CMOS circuit is much smaller than the heater itself (i.e., high power efficiency).

Fig. 6 shows our heater controller circuit design to ensure maximum driver efficiency. We utilized a switch-mode driver comprising of a single nMOS switch connected to the heater. Since the voltage swing of the heater is only 3.3 V, it was possible to directly use a thick-oxide device available in the CMOS process without cascoding (unlike [16]). The first-order $\Delta\Sigma$ modulator in the digital domain generates a PDM

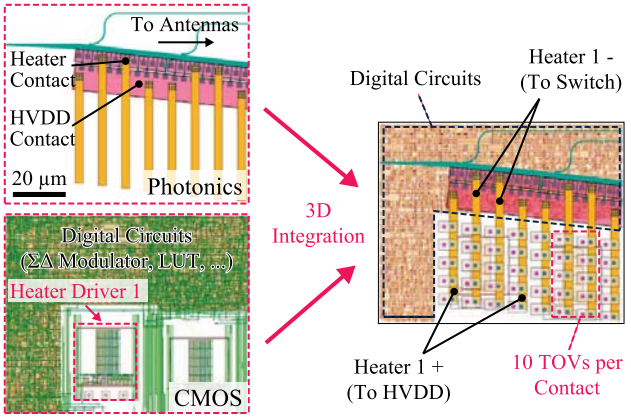


Fig. 7. Relative placement and TOV-based routing of the thermal phase shifter and the CMOS driver chain, surrounded by digital circuits including PDM modulators and on-chip LUT.

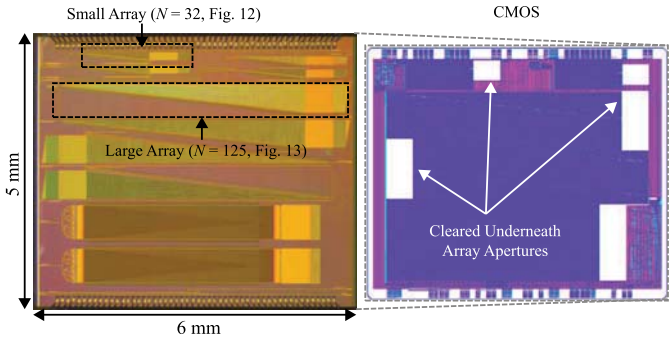


Fig. 8. Die micrograph of the OPA chip and the GDS image of the CMOS, located underneath the visible photonics layer.

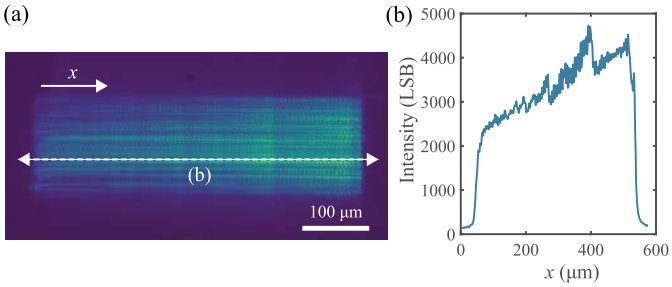


Fig. 9. (a) Near-field image of the illuminating small array aperture and (b) its cross section along the grating antenna.

signal [30] with 8-bit resolution to support an element count up to 128 with an extra bit for calibration, and the PDM signal drives the heater switch through a series of buffers and a level shifter. Modulated heater power is finally low-pass filtered and mapped to the heater temperature by the thermal frequency response. The driver chain was designed to support the maximum clock rate of ∼400 MHz so that the residual ripple of the PDM signal is sufficiently suppressed. The clock rate was ultimately limited by the current waveform duty cycle distortion caused by the finite edge rate of the switch input voltage (Fig. 6). In addition to higher efficiency, another advantage of the switch-mode driver with PDM modulation compared to a current-mode DAC is its inherent linearity. Since a nonreturn to zero (NRZ) signal is transferred from the driver input to the heater power instead of an analog signal, it completely circumvents the nonlinear relationship between the current and the heater temperature.

Fig. 7 shows how the heater and controller circuits are located in 3-D. Thanks to its simplicity, the resulting switch-mode driver front end is extremely compact (22 μm × 22 μm), which is smaller than the size of the phase shifter (32 μm long). This enabled us to place the driver front end directly underneath the heater in a pitch-matched fashion and limit the physical connection between the heater and nMOS switch to direct vertical TOV connections. This eliminates potential IR loss from extra wires, which can be a problem considering high heater current (up to 12.12 mA) due to low heater resistance. Ten TOVs per one connection (or 20 TOVs/heater) were used in parallel to ensure electromigration-free operation and further minimize IR loss. Finally, the remaining CMOS area was simply surrounded by the digital control circuitry through automatic place and route. The highly digital nature of our DAC design and flexible TOV connections also enable efficient utilization of the chip area with an overall floorplan matched to the size of the OPA in the photonic layers. This is particularly important in our 3-D integration platform since a significant portion of the silicon area would be wasted if the footprint of the CMOS and photonics is not matched.

CMOS power consumption is a function of clock rate and DAC input code. Even for a 400 MHz clock rate and the worst case DAC code of 0 (100% activity factor), the simulated CMOS power was 1.6 mW (1.4 mW in the driver chain, 234 μW in the PDM modulator), much smaller than the heater power. In reality, the measured thermal bandwidth was 32.3 kHz (Section V), and even for 11-bit resolution to support 1000 elements, ∼5 MHz clock rate (or ∼150 oversampling ratio) is sufficient (20 μW CMOS power).

V. Experimental Results

Fig. 8 shows the die micrograph of our OPA chip. It includes two types of OPAs composed of identical devices but with different element counts ($N = 32$ and $N = 125$) to demonstrate the scalability of the platform (further details and dimensions are shown in Figs. 12 and 13). The corresponding top-level layout of the CMOS layer is also shown. Note that the area underneath the array aperture was cleared during the design phase and later filled evenly with the regular density filling structure to eliminate unexpected stray light scattering from the CMOS side.

Fig. 9 shows the near-field image of the small array variant and the intensity cross section along the grating antenna. The intensity variation over the aperture was kept within 2.25 dB, confirming the effectiveness of the apodization technique illustrated in Section IV-A.

Characterization results for the phase shifter and controller circuit are presented in Fig. 10. As can be seen from the power versus DAC code plot [Fig. 10(a)], the step size is more compressed in the high power regime due to the increased heater resistance from temperature shift. Still, an approximately 40-mW range is achieved, which is sufficient for a 2π

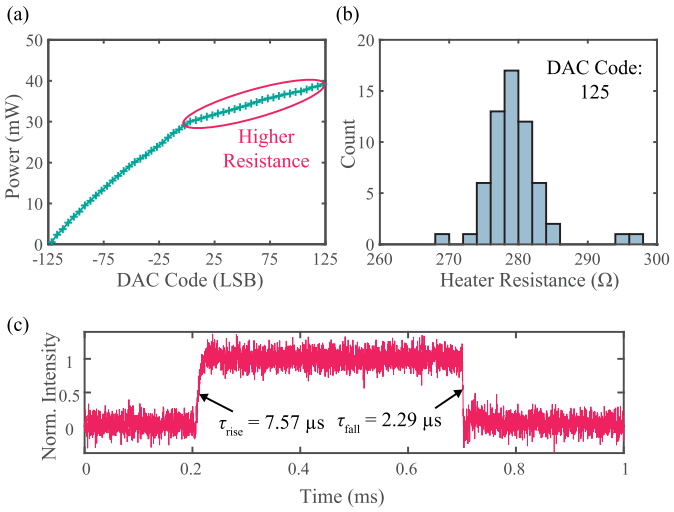


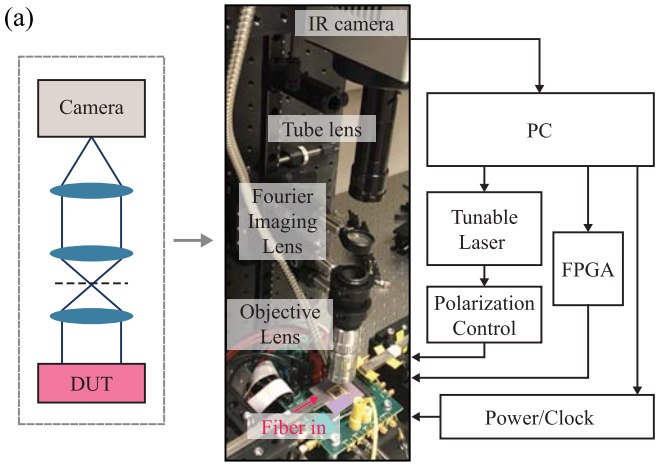
Fig. 10. Measurement results of the DAC and heater. (a) Power versus DAC code. (b) Statistics of the heater resistance. (c) Thermal transient response.

phase shift. Also, the heater resistance is close to the expected value of 270 Ω even if the resistance is slightly increased in the high power range [Fig. 10(b)], again due to the temperature dependence.

The transient response of the heaters is also characterized [Fig. 10(c)] using a setup where the heaters are driven by a square wave from a waveform generator, while a photodetector is aligned with the beam direction corresponding to one of the voltage levels, and the photodetector output is monitored on an oscilloscope. Note that the heater temperature and the photodetector output may have a nonlinear relationship depending on the beam shape and the size of the photodetector aperture. To minimize the impact of this potential nonlinearity, the amplitude of the square wave was lowered until it maintained a consistent edge shape while still showing sufficient extinction ratio. The average time constant from the cooling and heating transitions was 4.94 µs, corresponding to 32.3 kHz bandwidth assuming a single-pole response.

Fig. 11(a) shows the bench-top setup for characterizing the performance of an OPA and also for controlling the on-chip phase shifters. The far-field intensity pattern of the emitted light is directly captured on an IR camera (320 × 256 pixels at 30 µm pitch) through a standard three-lens Fourier imaging setup. The chip surface is placed at the working distance of the 10× or 20× infinity-corrected objective lens (f = 20 mm or 10 mm), and the telecentric setup formed by the Fourier imaging lens (f = 100 mm) focused on the back focal plane of the objective, and the tube lens (f = 200 mm) forms an image of the Fourier plane at the camera sensor (e.g., 27.5° × 22° field-of-view and 0.086° per pixel for the 20× objective). The resulting image is then streamed into the PC, which also controls the tunable laser, power/clock source, and the field-programmable gate array (FPGA) that programs the on-chip LUT that stores the phase shifter DAC codes via a serial interface.

Using the setup in Fig. 11(a), we can also carry out the array calibration to adjust the DAC LUT for optimum beam



(b)

```
Pick desired beam position coordinate
Set initial DAC inputs
while i < maximum iteration count do
  for n ← 1 to N do
    for ϵ ∈ {···, −Δ_i, 0, +Δ_i, ···} do
      DAC_{n,i} ← DAC_{n,i−1} + ϵ
      Measure beam quality
    end for
    Pick ϵ_best with maximum beam quality
    DAC_{n,i} ← DAC_{n,i−1} + ϵ_best
  end for
end while
```

Fig. 11. (a) Experimental setup including far-field imaging optics. (b) Pseudocode of the local search-based beam calibration process.

quality. Fig. 11(b) shows the pseudocode of the simple local search algorithm used for OPA calibration. It starts from the first phase shifter in the bus waveguide, adjusts its DAC input until it finds the code that maximizes the target beam quality [e.g., the sidelobe suppression ratio (SLSR) or foreground–background ratio, both of which can be extracted from the IR image], and then moves on to the next phase shifter. The camera image was averaged from multiple shots to minimize the impact of readout noise. Once it reaches the final phase shifter, one iteration cycle is done. Each step took about a minute on average, largely limited by the camera-PC interface and FPGA-PC interface for LUT configuration, which was implemented using a generic API and python script. This can be improved in the future by writing custom software and firmware to streamline the data movement. In the data presented in this article, two iteration cycles were performed using SLSR as the optimization target metric.

The impact of the beam calibration is highlighted in Fig. 12. In this example, the smaller variant with 32 elements (aperture size: 0.5 mm × 0.13 mm) is used. The beam is tightly focused in the ϕ-direction (FWHM$_\phi$ ≈ 0.15°) and almost identical to the expected beamwidth for a 0.5-mm aperture and λ = 1530 nm, again confirming wide effective aperture and the validity of the apodized antenna design. However, without array calibration, significant sidelobe and limited beam

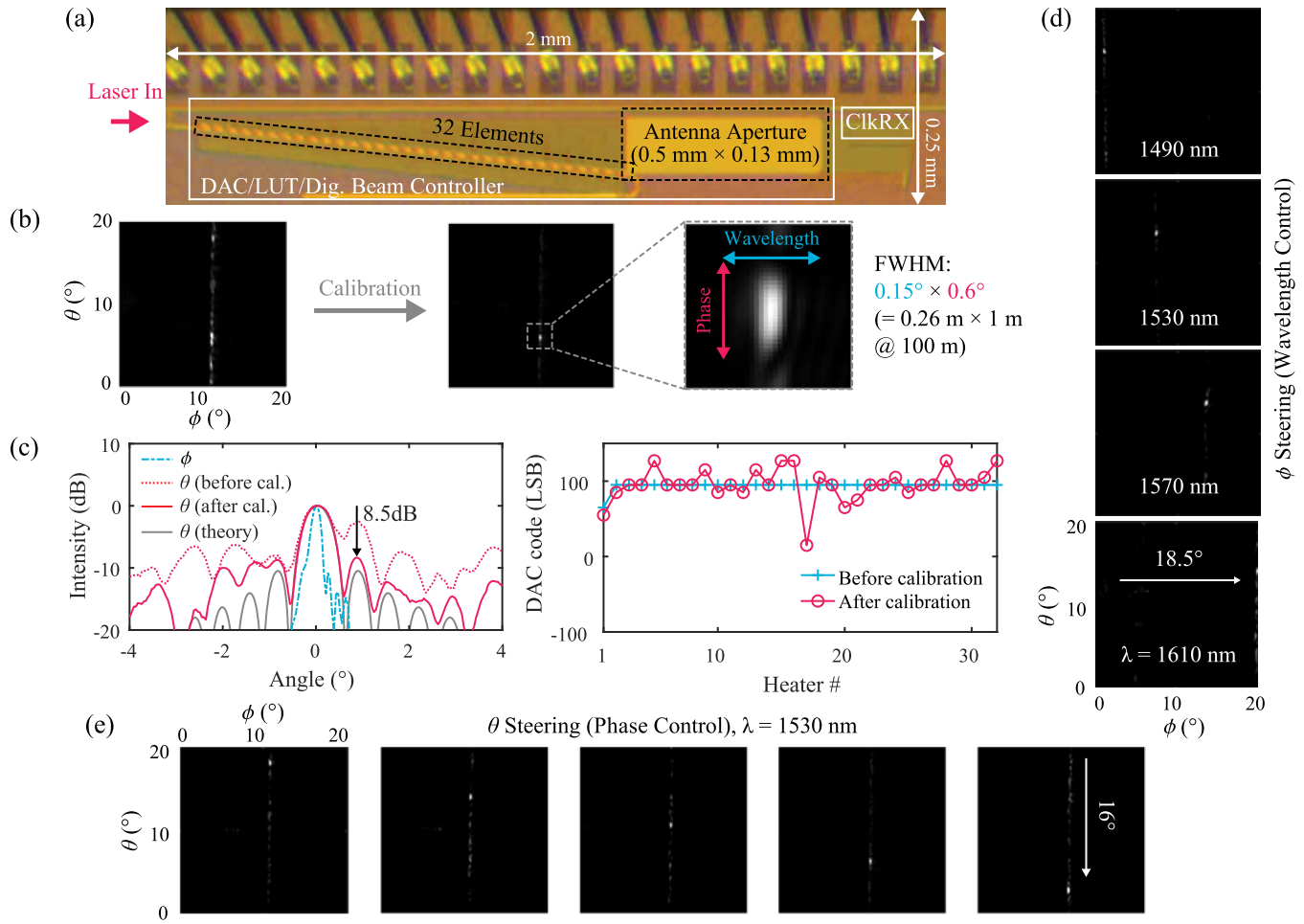


Fig. 12. Demonstration of beam calibration performance and beam-steering capability for the OPA with 32 elements. (a) Detailed die micrograph of the 32-element phased array. (b) Far-field image of the array, before and after calibration. (c) Cross section of (b) along ϕ and θ, as well as the DAC code distributions. (d) and (e) Beam-steering along ϕ and θ through laser wavelength and on-chip phase shifter control.

contrast in θ is clearly observed from the far-field intensity image as well as the dotted line in the cross-sectional plot. After calibration, the beam quality is significantly improved, achieving SLSR of 8.5 dB. Fig. 12 also shows a full 2-D beam-steering demonstration based on the same calibration process with two iterations at each beam position, over 16° in θ via phase shifter control and over 18.5° in ϕ by tuning the input laser wavelength across a 120-nm range centered around 1550 nm. Again, the steering range in θ can potentially be extended by reducing the antenna pitch (e.g., 56° was demonstrated in [31]). A final beamwidth of $\text{FWHM}_\phi \times \text{FWHM}_\theta = 0.15° \times 0.6°$ is achieved, which corresponds to a lateral resolution of 0.26 m × 1 m at 100-m range.

Since our OPA is completely integrated into a single chip through a 3-D integration process and enables a pitch-matched layout design of phase shifters and control circuitry, further OPA scaling implies nothing other than additional silicon area and comes with zero overhead for I/O support or electronics routing/placement, as shown in the large array demonstration result, shown in Fig. 13. The antenna aperture size of this large array demonstration is four times larger (0.5 mm × 0.5 mm), which results in a measured FWHM beamwidth after phase shifter calibration of 0.15° × 0.25° (matching approximately 0.1°–0.2° beamwidth requirements of long-range automotive LiDAR systems).

Table I summarizes our results and compares them with state-of-the-art OPA implementations designed for beam-steering. The first four columns of the table compare our results with the single-chip OPA tailored for wide-range beam-steering [15]. The next five columns present the latest multi-chip or photonics-only examples. Among single-chip demonstrations, our work is the first that can do full 2-D steering with reasonable range via phase and wavelength control and with high beam resolution in both dimensions.

VI. Future Directions

Based on the discussion so far, at least in terms of beam resolution and steering range, we conclude that an OPA-based low-cost solid-state beam scanner is becoming a reality. However, the basic requirements discussed in Section II-A tell only one side of the story; to be successfully deployed in real systems, one should also consider metrics related to reliability and maximum emission power.

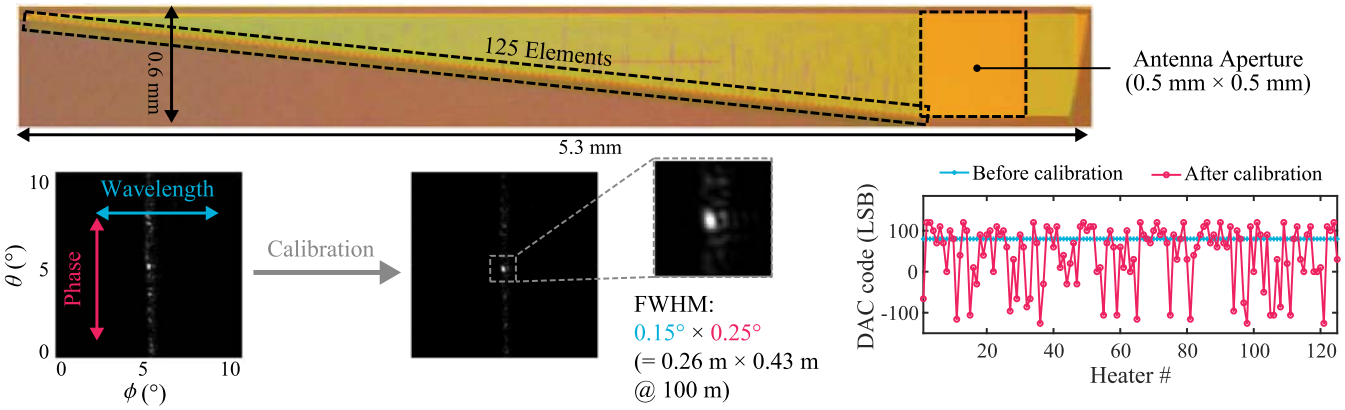


Fig. 13. View of the larger 125 element array and calibrated beam performance.

TABLE I
SUMMARY AND COMPARISONS WITH PRIOR BEAM-STEERING OPAS

	This Work		[15]		[31]	[14]	[13]	[32]	[16]
	Small Variant	Large Variant	Small Variant	Large Variant					
Technology	Silicon Photonics/ 65nm CMOS		0.18 µm SOI CMOS		Silicon Photonics	Silicon Photonics	Silicon Photonics	Hybrid III-V/ Si-Photonics	Silicon Photonics
Electronics	Integrated DAC		Integrated DAC		External	External	External	External	External CMOS
Beamwidth (ϕ/θ)	0.15°/0.6°	0.15°/0.25°	>10°/1.2°	>10°/0.03°	0.04°/0.04°	0.15°/0.15°	0.14°/0.14°	0.6°/1°	0.8°/0.8°
Aperture Size	500 µm× 130 µm	500 µm× 500 µm	3.55 µm× 64 µm	3.55 µm× 2046 µm	2000 µm× 2000 µm	1000 µm× 665 µm	910 µm× 910 µm	N/A	N/A
Steering Range (ϕ/θ)	18.5°/16°	-/-	0°/45°	0°/-	15°/56°	14°/70°	17°/80°	3.6°/23°	16°/16°
Sidelobe Suppression	8.5 dB	7.4 dB	9 dB	9 dB	12 dB	8 dB	9 dB	5.5 dB	12 dB
Number of Elements	32	125	32	1024	512	512	128	32	128
Independent Phase Controls	32	125	36	136	512	512	128	32	128
Phase Shifter Type	Thermal		Thermal		Electro-Optic	Thermal	Thermal	Thermal/ Electro-Optic	Thermal
Phase Efficiency	20 mW/π		34.7 mW/π		<2 µW/π	2.6 mW/π	80 mW/π	160 mW/π	10.6 mW/π
Required Voltage Supply	3.3 V		8 V		N/A	N/A	N/A	N/A	10 V

Ensuring robust operation against temperature variation is particularly important for automotive applications. According to the industry standard [33], consistent operation across −40°C–+105°C is a minimum requirement. Due to the same thermooptic effect, we utilized to build phase shifters, on-chip waveguides will undergo significant index shift in the presence of ambient temperature variation. Fortunately, the impact of ambient temperature shift is common to on-chip waveguides, and the relative phase difference between antennas, which affects the actual beam pattern, is largely unaffected.

One notable exception is the case where the optical distribution network introduces physical path length mismatch. For instance, distribution through cascaded evanescent coupling used in this article or for the sub-row distribution in [15] can cause phase slope bias when temperature changes, which results in beam direction offset. Path mismatch can be primarily removed through the careful layout. For the cascaded coupler structure, the optical path after the directional coupler up to the antenna should gradually decrease so that it cancels the additional delay in the bus waveguide. Alternatively,

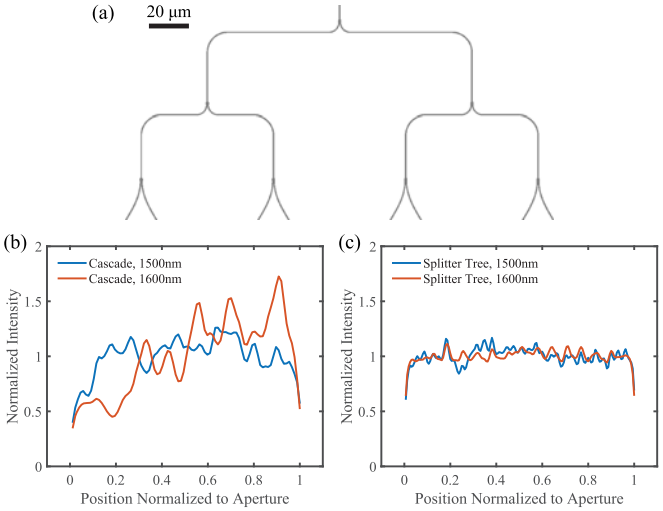


Fig. 14. (a) Layout of 1 × 2 splitter-based optical distribution tree available in our process. (b) Measured power distribution across the cascaded directional coupler-based OPA at 1500- and 1600-nm wavelength. (c) Same data as (b), but from the OPA with the distribution using the design in (a).

an inherently symmetric distribution architecture can be used. For example, a tree of 1×2 splitters shown in Fig. 14(a) [15], [34] ensures precise match from the OPA input to individual antennas. Moreover, a splitter tree can maintain even power distribution over a wider range of wavelengths compared to the cascaded directional coupler, as shown by the measurement results from our test structures [Fig. 14(b)].

From (4), one can also note that the emission angle of the grating antenna is also subject to absolute effective index, which makes it temperature sensitive. A change in material can resolve the issue: since our integration platform enables photonics process customization, it is possible to replace the silicon-based antennas in the OPA with antennas based on a material with a lower thermooptic coefficient, such as silicon nitride (a similar grating design based on SiN was demonstrated in [34]).

To be used in long range (200–300 m) applications, it is also desired that the OPA can support the maximum permissible radiation power set by the laser safety regulation (∼10 dBm for IEC60825-1 Class 1 in C-band [20]). In our prototype, the fiber-to-chip edge coupler has ∼ 3 dB loss, and the theoretical emission efficiency ($\eta = P_{\text{beam}}/P_{\text{input}}$) for the 2-D array ($N = 125$, $d = 4$ μm, $d_{\text{grating}} = 700$ nm, $l_{\text{grating}} = 500$ μm) calculated from the basic array directivity equation in [35] and single antenna gain extracted from Fig. 4(c) is ∼ −9 dB. Considering 3 dB/cm waveguide loss and a 5-mm-long distribution network (Fig. 13), the overall insertion loss is expected to be at least 13.5 dB. Even with a reduced antenna spacing (e.g., $d = 2$ μm) and unidirectional antenna design [29] to improve the efficiency by 6 dB, ∼20 dBm of optical power is needed at the OPA input to support ∼10 dBm beam despite extra loss from couplers and phase shifters. It is well known that silicon waveguides are unable to handle more than ∼10 dBm without exhibiting significant loss due to two-photon absorption (TPA) [36]. SiN integration can also resolve this issue since SiN can handle much higher power density [34].

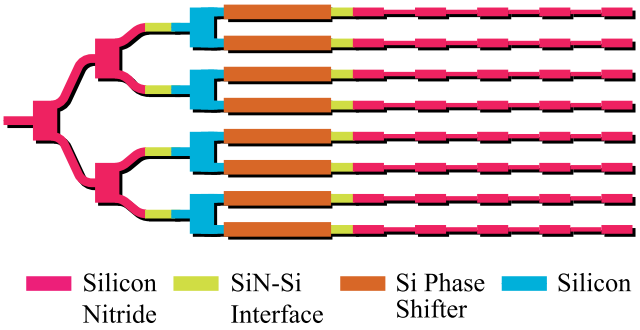


Fig. 15. Proposed temperature-insensitive, high-emission power OPA architecture realizable in our platform through process customization.

Fig. 15 shows a high-emission power OPA architecture with reliable operation against temperature drift, realizable in our platform. High power density at the input and first few stages of splitter tree are handled by SiN waveguides.

Meanwhile, although a bench-top laser was used in this article, a deployable system would eventually include an integrated laser that can support sufficient output power and wide wavelength tuning range (50–100 nm) to enable 2-D steering. Fortunately, a variety of lasers based on compound materials originally developed for *C*-band fiber optic communications can be re-branded for free-space optics [37]. In particular, III/V semiconductor lasers with large tuning range [38] and high output power [39] are promising because they can be heterogeneously integrated with silicon photonics, removing fiber-to-waveguide coupler loss. Alternatively, rare-earth-doped lasers [40] with high output powers over 300 mW [41] and wide tunability over 46 nm [42] can be utilized to further minimize the unit cost. Although it involves an additional optical pump, the integration process is much simpler and done at the wafer scale.

Finally, the simple local search-based calibration algorithm used in this article may not be practical for larger element counts and may fail to find the global optimum within a reasonable time. In fact, characterizing random phase fluctuations in OPAs, is an equivalent problem to acquiring a phase image at the array aperture. Using a near-field image of the intensity distribution at the aperture and a far-field image showing the Fourier image of the wavefront as two inputs, standard phase retrieval algorithms, such as the Gerchberg–Saxton algorithm [43], can be applied to potentially enable one-shot calibration.

VII. Conclusion

In order for integrated OPAs to be a reliable solid-state alternative to mechanical beam scanners, the technology must support 500–1000 elements in spite of stringent area/power/cost constraints. To resolve I/O and electronics density problem, we proposed an OPA design based on a wafer-scale 3-D photonics/CMOS integration platform. With device and circuit designs that actively utilize flexible, dense TOV connections between photonics and CMOS, we have demonstrated a compact single-chip OPA with wide-range 2-D beam-steering and array scalability beyond 100s of elements. Our array calibration result also highlights the importance of

flexible phase control in achieving robust OPA performance, especially for thermooptic phase shifter designs that can facilitate compact, efficient control circuits suitable for large-scale OPAs. Furthermore, 3-D integration allows the photonics to be highly customized independent of electronics for target applications (e.g., *C*-band coherent optical receiver utilizing Ge photodiodes [44] and hybrid laser/optical gain [40], [42]), opening up unlimited opportunities for integrated free-space system design.

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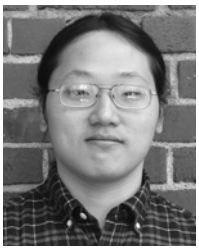

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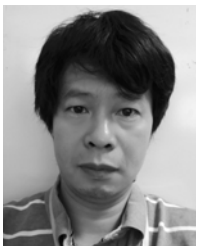

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