



SEMulator3D®: Speeding up Process Optimization with Virtual Processing

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Abstract: Advanced CMOS scaling and new memory technologies have introduced increasingly complex structures into the device manufacturing process. For example, the increase in NAND memory layers has achieved greater vertical NAND scaling and higher memory density but has led to challenges in high aspect ratio etch patterning and footprint scaling issues. Unique integration and patterning schemes have been employed to solve these scaling challenges, but they create additional design rule challenges. Two-dimensional (2D) design rule checks (DRCs) are no longer sufficient to achieve performance and yield goals, due to the 3D nature of modern semiconductor devices. Design of Experiments (DOEs) for process characterization and optimization, traditionally used to save time and cost in developing process recipes, now require hundreds of physical experiments involving significant off-process time and substantial wafer testing. Moreover, non-intuitive interactions among process steps, as well as tightening process windows, have made it difficult to deliver concurrent performance and yield optimization using first principle modeling approaches. A 3D understanding of complex process sequences is required to solve these scaling challenges, and is provided by Coventor SEMulator3D®, a virtual fabrication modeling platform.

Bio: Dr. Joseph Ervin is the Director of the Semiconductor Process and Integration group at Coventor, where he is responsible for managing the support of Coventor's Virtual Fabrication platform. Previously, he worked for IBM on semiconductor device and integration development at multiple research and foundry locations, including ST Microelectronics, the College of Nanoscale Science and Engineering, and at GlobalFoundries. His current position involves managing customer applications for our next node semiconductor integration challenges, along with development of unique methods for modeling and solving these issues. He holds a Ph.D. in Device Physics from Arizona State University.