betr

Berkeley Emerging Technologies Research Center

Annual Report

June 2020 – May 2021

Questions regarding this report or requests for additional information should be directed to:

Michael H. Bartl
Executive Director
Berkeley Emerging Technologies Research (BETR) Center
University of California, Berkeley
Office: 510-664-7814
Mobile: 213-400-5895
Email: mbartl@berkeley.edu

Table of Contents (with clickable direct-links)

1 The Berkeley Emerging Technologies Research Center 5

1.1 Executive Statement 5

1.2 Leadership Team 6

1.3 Corporate Membership 13

2 Research Activities 15

2.1 Motivation and Overview 15

2.2 Millivolt Switches 16

2.2.1 Recent Achievements 16

2.2.2 Current Projects 18

2.2.3 Publications (MS) 19

2.3 Embedded Memory 20

2.3.1 Recent Achievements 20

2.3.2 Current Projects 23

2.3.3 Publications (EM) 24

2.4 Flexible and Wearable Electronics 25

2.4.1 Recent Achievements 25

2.4.2 Current Projects 27

2.4.3 Publications (FE) 27

2.5 Hardware Accelerators for AI 28

2.5.1 Recent Achievements 28

2.5.2 Current Projects 30

2.5.3 Publications (AI) 32

2.6 System Integration 33

2.6.1 Recent Achievements 33

2.6.2 Current Projects 35

2.6.3 Publications (SI) 36

2.7 Computational Imaging 37

2.7.1 Recent Achievements 37

2.7.2 Current Projects 39

2.7.3 Publications (CI) 39

2.8 Optical Interconnects and Integration 40

2.8.1 Recent Achievements 40

2.8.2 Current Projects 42

2.8.3 Publications (OI) 44

3 Knowledge Transfer 45
3.1 Overview 45
3.2 BETR Center Workshops 46
3.3 Research Seminar/Webinar Series 49
3.4 Publications 51
3.5 Technology Transfer 58
3.5.1 Patents and Patent Applications 58
3.5.2 Available Technologies 59

4 Appendices 62
Appendix A: Abstracts of Research Seminars/Webinars 63
Appendix B: Agenda of 2020 Spring BETR Center Workshop 84
Appendix C: Agenda of 2020 Fall BETR Center Workshop 85

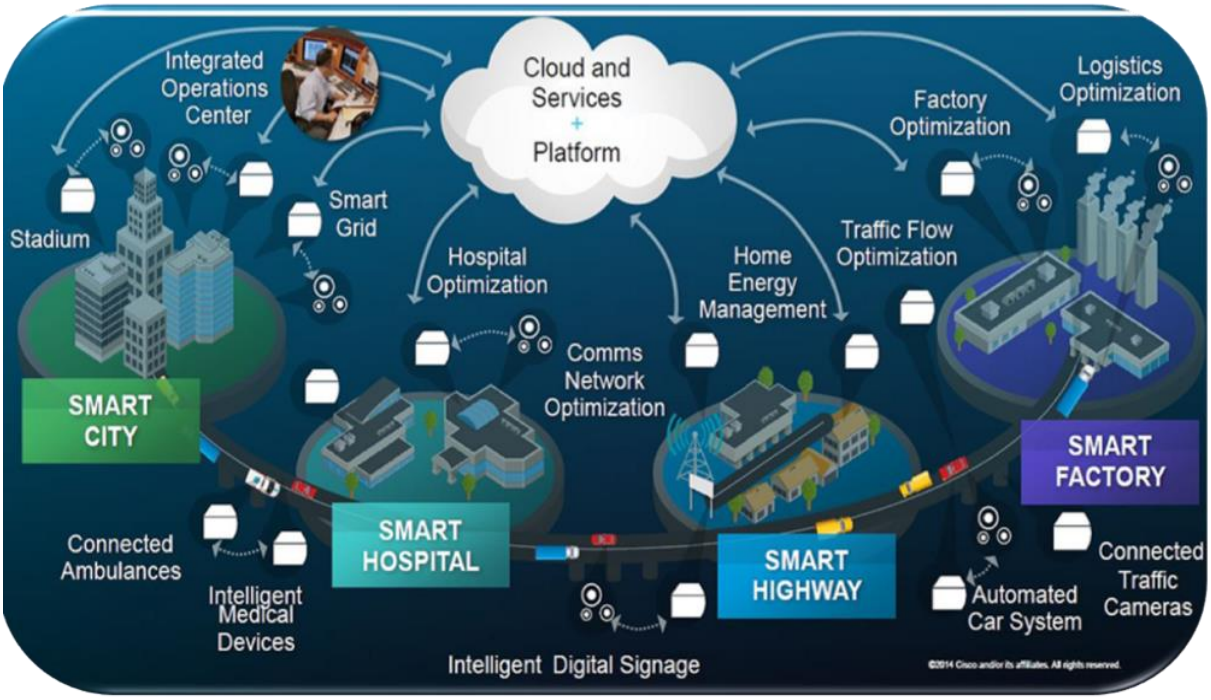
The Berkeley Emerging Technologies Research Center

1.1 Executive Statement

The Berkeley Emerging Technologies Research (BETR) Center is a hub of physical electronics research at the University of California, Berkeley. It serves as a nexus for interactions between faculty and student researchers and leading semiconductor companies for long-term research collaborations and knowledge transfer. Research activities in the BETR Center encompass a wide range from the search for new materials and manufacturing processes to the development of novel computing and memory devices and the design of heterogeneous integrated systems.

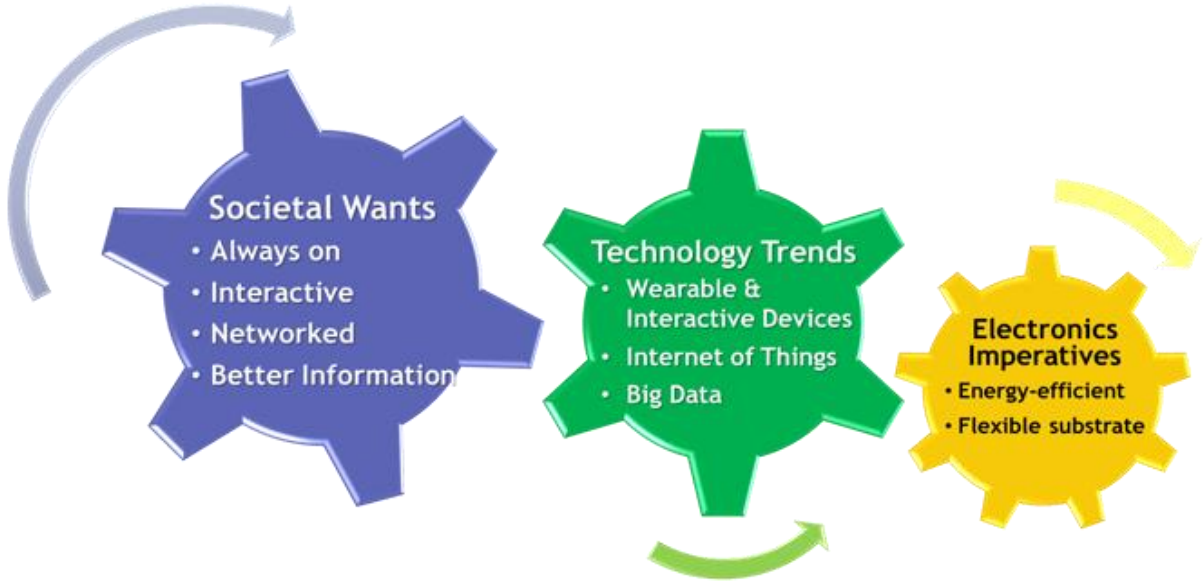
The mission of the BETR Center is to foster innovation in materials, processes and devices toward the vision of ubiquitous information systems for enhancing health and quality of life in our global society.

For the last five decades, steady miniaturization of the transistor has yielded continual improvements in integrated-circuit performance and cost per function, with dramatic impact on virtually every aspect of life in modern society. This proliferation of information and communication technologies has enabled cloud computing and the Internet of Things, which together with recent advancements in machine learning give rise to the vision of an *artificially intelligent world* with systems for coordinating critical infrastructure for *smart cities*, managing personalized health care and medicine for *smart hospitals*, automating vehicles and traffic flow for *smart highways*, and optimizing manufacturing and logistics for *smart factories*.



The real-time processing of large quantities of data required by artificially intelligent systems is possible today because of the dramatic improvement of the capabilities of computing devices. This exponential increase of computation power in the last 120 years is described in Kurzweil's Law, which predicts that computing systems are rapidly approaching the capability of the human brain. Underlying Kurzweil's Law is Moore's Law, describing the evolution of transistors fueled by advancements in materials, processes, and structures that have enabled transistors to be miniaturized to sub-20 nm feature sizes in the most advanced chips today. However, as fundamental limits are approached, transistor scaling will not be as straightforward in the future as it has been in the past. Alternative approaches for improving chip functionality, cost per function and energy efficiency eventually will thus be necessary to sustain the rapid growth of the semiconductor industry beyond the next decade.

The BETR Center is ideally positioned to address these challenges by bringing together a broad range of world-renowned leaders in electronic devices and technology research. The BETR team of UC Berkeley professors, postdocs, and students collaborates across the disciplines of electrical engineering, computer science and materials science to build the technological foundation for future ubiquitous information systems. Considering that artificially intelligent systems must always be awake, interactive, and networked across many devices, it is imperative that future electronic systems are more energy efficient in order to be ubiquitous, and they need to be compatible with flexible substrates to be wearable.



1.2 Leadership Team

To meet the need for a new industry growth paradigm (beyond Moore's Law), the BETR Center brings together research leaders whose collective expertise spans not only materials, structures and manufacturing processes for nanoelectronics, nanomagnetics, nanophotonics and optoelectronics

but also computational imaging and metrology, and IC design and system architecture. In fact, BETR faculty co-directors have contributed significant innovations to sustain Moore's Law in the last few decades, including the development of "spacer lithography" (also known as self-aligned double patterning, SADP) for patterning of sub-lithographic features, the "FinFET" (a fin-shaped field-effect transistor structure) for transistor scaling to below 10 nm, and most recently the "negative capacitance FET" (comprising a ferroelectric-dielectric bilayer gate-insulating film) to reduce transistor operating voltage.

Faculty co-Directors *(in alphabetical order)*

Ana Claudia Arias

Printed and Flexible Electronics

Dr. Ana Claudia Arias is a professor in the Department of Electrical Engineering and Computer Science at UC Berkeley. She received her Ph.D. in Physics from the University of Cambridge, UK in 2001. Prior to that, she received her master's and bachelor's degrees in physics from the Federal University of Paraná in Curitiba, Brazil in 1997 and 1995, respectively.

Dr. Arias joined the University of California, Berkeley in January of 2011. Before that she was manager of the Printed Electronic Devices Area and a Member of Research Staff at PARC, a Xerox Company. She went to PARC, in 2003, from Plastic Logic in Cambridge, UK where she led the semiconductor group. Her research focuses on the use of electronic materials processed from solution in flexible electronic systems. Dr. Arias uses printing techniques to fabricate flexible large area electronic devices and sensors.

Jeffrey Bokor

Embedded Memory, Millivolt Switches, Integrated Systems

Dr. Jeffrey Bokor is the Paul R. Gray Distinguished Professor of Engineering in the Department of Electrical Engineering and Computer Sciences at UC Berkeley, with a joint appointment as Senior Scientist in the Materials Science Division at Lawrence Berkeley National Laboratory. Currently, he also serves as Chair of the Electrical Engineering and Computer Sciences Department.

Dr. Bokor received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology in 1975, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1976 and 1980, respectively. From 1980 to 1993, he was at AT&T Bell Laboratories where he did research on a variety of topics in laser science, advanced lithography for integrated circuits, as well as semiconductor physics and technology, and held several management positions.

Dr. Bokor joined the Berkeley faculty in 1993. His current research activities include nanomagnetics/spintronics, graphene electronics, nanophotonics, and nano-electromechanical systems. He is a fellow of IEEE, APS, and OSA.

Ali Javey

Flexible Electronics, Millivolt Switches

Dr. Ali Javey is the Lam Research Distinguished Chair in Semiconductor Processing and a professor of Electrical Engineering and Computer Sciences at UC Berkeley. He is also a senior faculty scientist at the Lawrence Berkeley National Laboratory where he serves as the program leader of Electronic Materials (E-Mat). He is a co-director of Berkeley Sensor and Actuator Center (BSAC) and an associate editor of ACS Nano.

Dr. Javey received a Ph.D. degree in chemistry from Stanford University in 2005 and was a Junior Fellow of the Harvard Society of Fellows from 2005 to 2006 before joining the faculty at UC Berkeley. His research interests encompass the fields of chemistry, materials science, and electrical engineering and focus on the integration of nanoscale electronic materials for various technological applications, including low power electronics, flexible circuits and sensors, and energy generation and harvesting.

Dr. Javey is the recipient of numerous awards, including the Dan Maydan Prize in Nanoscience Research, the MRS Outstanding Young Investigator Award, the Nano Letters Young Investigator Lectureship, the National Academy of Sciences Award for Initiatives in Research, Technology Review TR35, and the NSF Early CAREER Award.

Tsu-Jae King Liu

Millivolt Switches, Embedded Memory, Integrated Systems,

Dr. Tsu-Jae King Liu is the Dean of the College of Engineering and the Roy W. Carlson Professor of Engineering at UC Berkeley. Previously, she served as Chair of the EECS Department, Associate Dean for Research in the College of Engineering, and Faculty Director of the Marvell Nanofabrication Laboratory. She was also Senior Director of Engineering in the Advanced Technology Group of Synopsys, Inc. (2004-2006).

She received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from Stanford University. She joined the Xerox Palo Alto Research Center as a Member of Research Staff in 1992, to research and develop high-performance thin-film transistor technologies for flat-panel display applications. In 1996 she joined the faculty at UC Berkeley. Her research activities are presently in advanced materials, fabrication processes and devices for energy-efficient electronics. She has authored or co-authored over 550 publications and holds over 95 patents.

Dr. Liu's awards include the DARPA Significant Technical Achievement Award for development of the FinFET, the IEEE Kiyo Tomiyasu Award, the Intel Outstanding Researcher in Nanotechnology Award, and the Semiconductor Research Corporation (SRC) Aristotle Award. Dr. Liu is a Fellow of the IEEE and a member of the U.S. National Academy of Engineering, and she serves on the Board of Directors for Intel Corporation and on the Board of Directors for MaxLinear, Inc.

Ramamoorthy Ramesh

Spin-Based Logic, Embedded Memory

Dr. Ramesh is the Purnendu Chatterjee Chair Professor in Materials Science and Physics at UC Berkeley, and a Faculty Senior Scientist at Lawrence Berkeley National Laboratory. He pursues key materials physics and technological problems in complex multifunctional oxides. Using conducting oxides, he solved the 30-year enigma of polarization fatigue in ferroelectrics. He pioneered research into manganites coining the term, Colossal Magnetoresistive (CMR) Oxides. His work on multiferroics demonstrated electric field control of ferromagnetism, a critical step towards ultralow power memory and logic elements. His extensive publications on the synthesis and materials physics of complex oxides are highly cited (over 65,000 citations, H-factor =144).

He is a fellow of APS, AAAS & MRS and an elected member of the U.S. National Academy of Engineering and a Foreign member of the Royal Society of London. His awards include the Humboldt Senior Scientist Prize, the APS Adler Lectureship and McGroddy New Materials Prize, the TMS Bardeen Prize and the IUPAP Magnetism Prize and Neel Medal. He was recognized as a Thomson-Reuters Citation Laureate in Physics for his work on multiferroics.

He served as the Founding Director of the successful Department of Energy SunShot Initiative in the Obama administration, envisioning and coordinating the R&D funding of the U.S. Solar Program, spearheading the reduction in the cost of Solar Energy. He also served as the Deputy Director of Oak Ridge National Laboratory and the Associate Lab Director at LBNL.

Sayeef Salahuddin

Embedded Memory, Accelerators for AI, Millivolt Switches

Dr. Sayeef Salahuddin is the TSMC Distinguished Professor of Electrical Engineering and Computer Sciences at UC Berkeley. He is the co-director of the Berkeley Center for Negative Capacitance Transistors (BCNCT) and the Berkeley Device Modeling Center (BDMC), and he is an associate director of ASCENT, a multi-university research center within the DARPA/SRC JUMP initiative.

His research lab explores the conceptualization and demonstration of novel device physics for logic and memory applications. Dr. Salahuddin is widely known for his discovery of the Negative Capacitance phenomenon in ferroelectric materials.

Dr. Salahuddin has received the Presidential Early Career Award for Scientist and Engineers (PECASE), the highest honor bestowed by the US Government on early career scientists and engineers. He also received a number of other awards including the NSF CAREER award, the IEEE Nanotechnology Early Career Award, the Young Investigator Awards from the AFOSR and ARO and the IEEE George Smith Award. He is a Fellow of the IEEE and the APS.

Sophia Shao

Accelerators for AI

Dr. Sophia Shao is an Assistant Professor and an SK Hynix Faculty Fellow in the Electrical Engineering and Computer Sciences department at UC Berkeley. Previously, she was a Senior Research Scientist at NVIDIA Research.

Dr. Shao received her Ph.D. degree in 2016 and S.M. degree in 2014 from Harvard University. Her research interests are in the area of computer architecture, with a special focus on specialized accelerator, heterogeneous architecture, and agile VLSI design methodology.

Dr. Shao's work has been awarded a Best Paper Award (MICRO 2019) and Top Picks in Computer Architecture (2014). Her Ph.D. dissertation was nominated by Harvard for ACM Doctoral Dissertation Award. Dr. Shao is a Siebel Scholar, an invited participant at the Rising Stars in Electrical Engineering and Computer Science Workshop, and a recipient of the IBM Ph.D. Fellowship.

Vladimir Stojanović

Accelerators for AI, Optical Interconnects, Integrated Systems

Dr. Vladimir Stojanović is Professor of Electrical Engineering and Computer Science at UC Berkeley. He received his Ph.D. in Electrical Engineering from Stanford University in 2005, and the Dipl. Ing. degree from the University of Belgrade, Serbia in 1998. He was also with Rambus, Inc., Los Altos, CA, from 2001 through 2004 and with MIT as Associate Professor from 2005 to 2013.

Research interests of Dr. Stojanović include design, modeling and optimization of integrated systems, from CMOS-based VLSI blocks and interfaces to system design with emerging devices like NEM relays and silicon-photonics. He is also interested in design and implementation of energy-efficient electrical and optical networks, and digital communication techniques in high-speed interfaces and high-speed mixed-signal IC design.

Dr. Stojanović received the IBM Faculty Partnership Award, the NSF CAREER Award, the ICCAD William J. McCalla, the IEEE Transactions on Advanced Packaging, and the ISSCC Jack Raper best paper award. He was an IEEE Solid-State Circuits Society Distinguished Lecturer for the 2012-2013 term.

Laura Waller

Computational Microscopy

Dr. Laura Waller is an Associate Professor of Electrical Engineering and Computer Science at UC Berkeley, leading the Computational Imaging Lab. She is a Senior Fellow at the Berkeley Institute of Data Science (BIDS), with affiliations in Bioengineering and Applied Sciences & Technology. From 2016 to 2020 Dr. Waller held the UC Berkeley Ted Van Duzer Endowed Professorship.

Dr. Waller was a Postdoctoral Researcher and Lecturer of Physics at Princeton University from 2010-2012 and received B.S., M.Eng. and Ph.D. degrees from Massachusetts Institute of Technology in 2004, 2005 and 2010, respectively. She is a Moore Foundation Data-Driven Investigator, Bakar fellow, Distinguished Graduate Student Mentoring awardee, NSF CAREER awardee, Chan-Zuckerberg Biohub Investigator, SPIE Early Career Achievement Awardee and Packard Fellow.

Ming C. Wu

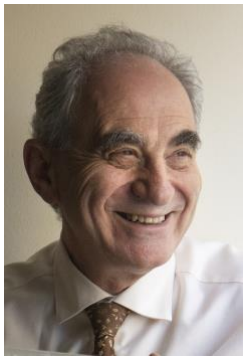
Photonics, Optical Interconnects, Accelerators for AI

Dr. Ming C. Wu is Nortel Distinguished Professor of Electrical Engineering and Computer Sciences and Co-Director of the Berkeley Sensor and Actuator Center (BSAC) and the Berkeley Emerging Technologies Research (BETR) Center at UC Berkeley. Dr. Wu received his B.S. degree in Electrical Engineering from National Taiwan University in 1983, and M.S. and Ph.D. degrees in Electrical Engineering and Computer Sciences from the University of California, Berkeley in 1986 and 1988, respectively.

From 1988 to 1992, he was Member of Technical Staff at AT&T Bell Laboratories, Murray Hill, New Jersey. From 1992 to 2004, he was Professor of Electrical Engineering at the University of California, Los Angeles (UCLA). He has been a faculty member at Berkeley since 2004.

His research interests include silicon photonics, optoelectronics, MEMS, MOEMS, and optofluidics. He has published 8 book chapters, over 600 papers in journals and conferences, holds 30 U.S. patents. His research has been successfully commercialized by OMM (MEMS optical switches, 1997) and Berkeley Lights (NASDAQ:BLI, optofluidics, 2011).

Prof. Wu is Fellow of IEEE and Optical Society (OSA), and a Packard Foundation Fellow (1992 – 1997). He was a member of the IEEE Photonics Society Board of Governors from 2013 to 2016. His work has been recognized by the 2016 IEEE Photonics Society William Streifer Scientific Achievement Award, the 2007 Paul F. Forman Engineering Excellence Award, the 2017 C.E.K. Mees Medal from the Optical Society (OSA), and the 2020 Robert Bosch Micro and Nano Electro Mechanical Systems Award from IEEE Electron Device Society.



Eli Yablonovitch

Millivolt Switches, Photonics, Accelerators for AI

Dr. Eli Yablonovitch holds the James & Katherine Lau Chair in Engineering in the Department of Electrical Engineering and Computer Sciences at UC Berkeley. He is also the Director of the NSF Science & Technology Center for Energy Efficient Electronics Science (E3S). Dr. Yablonovitch received his Ph.D. degree in Applied Physics from Harvard University in 1972. He worked for two years at Bell Telephone Laboratories, and then became a professor of Applied Physics at Harvard. He joined Exxon in 1979 and Bell Communications Research in 1984, before joining UCLA in 1992. Since 2007 he is a faculty member at UC Berkeley.

Prof. Yablonovitch introduced the idea that strained semiconductor lasers could have superior performance due to reduced valence band (hole) effective mass. With almost every human interaction with the internet, optical telecommunication occurs by strained semiconductor lasers. He is regarded as a Father of the Photonic BandGap concept, and he coined the term "Photonic Crystal". The geometrical structure of the first experimentally realized Photonic bandgap, is sometimes called "Yablonovite". In his photovoltaic research, Prof. Yablonovitch introduced the 4(n squared) ("Yablonovitch Limit") light-trapping factor that is in worldwide use, for almost all commercial solar panels. His mantra that "a great solar cell also needs to be a great LED", is the basis of the world record solar cells: single-junction 29.1% efficiency; dual-junction 31.5%; quadruple-junction 38.8% efficiency; all at 1 sun. Dr. Yablonovitch is elected as a Member of the National Academy of Engineering, the National Academy of Sciences, the National Academy of Inventors, the American Academy of Arts & Sciences, and is a Foreign Member of the Royal Society of London.

Executive Director

Michael H. Bartl

Center Administration

Dr. Michael H. Bartl is the executive director of the Berkeley Emerging Technology Research (BETR) Center and of the NSF Science & Technology Center for Energy Efficient Electronics Science (E^3S). Before moving to Berkeley, Dr. Bartl was a tenured faculty member at the University of Utah (where he still holds an appointment as research professor), and a visiting professor at the Technical University of Munich, Germany. He co-founded Navillum Nanotechnologies and published more than 65 papers about his research activities in functional nanostructured materials for energy and information technology applications.

A native of Austria, Dr. Bartl earned his doctorate in chemistry from Karl-Franzens University Graz before conducting postdoctoral research at the UC Santa Barbara. He was the recipient of a "DuPont Young Professorship", and he was named a Scialog Fellow by the Research Corporation for Science Advancement and a "Brilliant 10" researcher by Popular Science magazine.

1.3 Corporate Membership

The BETR Center was established with the goal to foster long-term academia-industry research collaborations and knowledge transfer by connecting UC Berkeley faculty and students who are building the technological foundation for future electronic devices and information systems with leading semiconductor companies. The BETR Center model of mutually beneficial collaborations gives corporate members early access to innovative ideas and research results, while university researchers gain insights into technological challenges faced by industry and society, and by seeing the results of their research applied to solve real-world problems. Moreover, the BETR Center provides various opportunities for member companies to interact directly with its faculty co-directors and 100+ graduate students and postdocs, many of whom are prospective future employees.

Since its inception in 2016, the BETR Center has seen a steady increase in the number of corporate members and we are delighted to currently have six leading companies in innovation in the semiconductor industry be part of the BETR Center. These companies are (in alphabetical order): Applied Materials, Atomera, Intel Corporation, Lam Research, SK Hynix, and TSMC.

Each of the member companies is represented in the BETR Center Technical Advisory Board (TAB). The TAB meets biannually as part of the BETR Center Workshops in a closed session to promote dialog between industry and academia. As such, the TAB is a crucial body in providing all BETR faculty co-directors important feedback for on-going research and future directions. Moreover, since the TAB comprises members from across the industrial ecosystem, it provides

BETR Center researchers with multiple and holistic perspectives. Additional benefits of a BETR Center corporate membership include:

Access to Periodic Research Webinars

During the fall and spring semesters, the BETR Center hosts a series of webinars featuring leading-edge research within the fields of physical electronics and optoelectronics. Given by researchers from UC Berkeley and other research institutions, these webinars are accessible via an online meeting service. Recordings of most of these webinars are made available to corporate members via password-protected access on the BETR website. In the last year, the BETR Center hosted and shared 20 research webinars (see Appendix A for details).

Attendance at Semi-Annual Research Reviews/Workshops

The BETR Center holds two research reviews/workshops per year in which the latest research results are presented. These events include oral presentations, industry panels, and lightning talks and poster sessions by BETR students and postdocs, offering an opportunity to meet and interact with student presenters, who are potential candidates for internships and/or employment. In the last year, two BETR Workshops were held (agendas for the spring and fall workshops are given as Appendix B and Appendix C, respectively).

Invitation to Berkeley EECS Annual Research Symposium (BEARS)

Each year in February, UC Berkeley's Department of Electrical Engineering and Computer Sciences hosts a day-long research conference featuring a variety of informative talks by distinguished faculty members and advanced graduate students. BEARS gives industrial affiliates a look at some of the most exciting research being pursued in information science and technology.

Customized Briefings

Upon request, the BETR Center staff will facilitate the scheduling of meetings with individual BETR Center co-directors. Based on best efforts, they will also facilitate introductions to other research centers and programs at UC Berkeley, as well as to companies that are part of UC Berkeley's technology innovation ecosystem.

Option to Direct Part of the Membership Contribution to a Faculty co-Director

Each corporate affiliate may direct part of the monetary membership contribution to specific research project(s) or research team(s). Typically, this is request is made at the start of the annual membership period. The BETR Center co-directors will then review requests and endeavor to allocate part of the contribution to support those research topics. Acknowledgment of the company's support will be made in all publication of the results from studies that are funded specifically by the allocated portion of the company's gift.

Facilitation of Technology Licensing

Twice a year, a list of research publications and patent applications will be provided to all industry affiliates. Upon request, the BETR Center staff will facilitate introductions to the Industry Alliances Office and Office of Technology Licensing at UC Berkeley for technology licensing.

2 Research Activities

2.1 Motivation and Overview

The central goal of the BETR Center is to provide solutions for driving innovation in materials, processes and solid-state devices to enable future ubiquitous information systems. Research activities are motivated by three main challenges for *ambient intelligence* to become a reality:

Looming Power Crisis for Computing: Electricity consumed by computing devices has increased exponentially with the proliferation of information and communication technology. To avoid a power crisis in the future, fundamentally new concepts for more energy-efficient logic switches and on-chip communication are needed. In addition to breakthroughs in solid-state science and technology, innovations in circuit design and system architecture will be necessary to avert a power crisis for computing.

Advent of the Internet of Things: The Internet of Things era of ubiquitous computing, wherein electronic devices are pervasive and wirelessly networked with access to cloud computing requires heterogeneous integration to diversify functionality and mechanical flexibility in mobile devices. For these to be affordable, new manufacturing techniques must be developed through interdisciplinary research into novel tools, processes, and materials that are compatible with low-cost plastic substrates.

Proliferation of Big Data Applications: "Big Data" has become the main driver for advances in memory technology and high-performance computing with increasing need for storing and processing large data sets in real-time to derive actionable information. Hardware innovations (including non-von-Neumann architectures) and new computational algorithms and software systems will be needed to meet the demand within reasonable energy and cost constraints.

Finding solutions to these grand challenges requires a concerted effort across disciplines and between academic and industrial researchers. In response, the BETR Center assembled a diverse group of UC Berkeley professors from electrical engineering, computer science and materials science, working with industry researchers, to build the technological foundation for future electronic devices and information systems. The BETR Center research teams are organized in six distinct, but highly collaborative, research thrusts (Figure 1): (1) Next-Generation Devices (including Millivolt Switches and Embedded Memory), (2) Flexible Electronics, (3) Accelerators for AI, (4) System Integration, (5) Optical Interconnects, (6) Metrology. In the following, information for each of the research thrusts is provided, including key achievements in the last twelve months and a description of current and future projects.

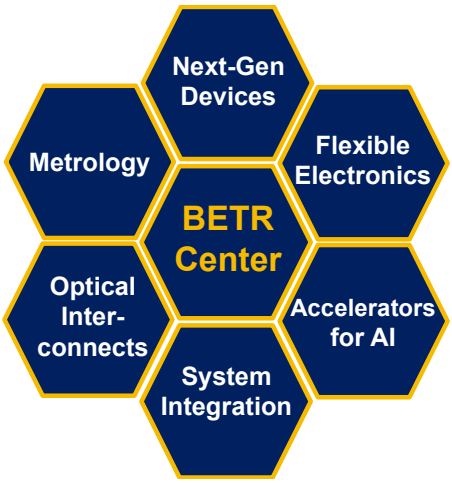


Figure 1. Research Thrusts of the BETR Center.

2.2 Millivolt Switches

*Research activities of the Millivolt Switches Thrust have been supported in part by directed membership contributions of **TSMC**, **SK Hynix**, and **Atomera**.*

Energy-efficient electronic devices are central to the BETR Center's research mission. Given recent advancements in cloud computing, social networking, mobile internet and data analytics, and the associated increase of battery-powered electronic systems, the development of intelligent systems that can operate at significantly reduced power consumption is now as relevant as ever. In fact, many of the ultra-low power electronics research projects in the BETR Center have originated in the Center for Energy Efficient Electronics Science (E^3S) based on the recognition that the energy used to manipulate a single bit of information is currently ~100,000 times greater than the theoretical limit. Research on ultra-low power devices and circuits in the BETR Center is conducted by **Professors Jeffrey Bokor**, **Ali Javey**, **Tsu-Jae King Liu**, **Sayeef Salahuddin**, and **Eli Yablonovitch**, and encompasses the search for alternatives to classical transistor-based digital logic. Examples include new circuit and system architectures leveraging zero-leakage nano-electromechanical (NEM) relays, field effect transistors (FETs) with 2D materials as active layers, graphene nanoribbon transistors, and current-driven ultra-fast nanomagnetic switches.[MS1-MS4]

2.2.1 Recent Achievements

A. Graphene Nanoribbons

Research on graphene nanoribbon (GNR) based millivolt switches in the BETR Center is led by the **Bokor** group (and Prof. Felix Fischer), in collaboration with BETR industry affiliate **TSMC**. The BETR team has successfully synthesized several distinct GNRs with ultra-narrow width (0.7-3.0 nm), atomically smooth edges and uniform bandgap. Furthermore, as shown in Figure 2 (left), fabrication processes were developed to integrate GNRs into functioning FETs with excellent switching behavior (ON/OFF ratios of ~10^5 and ON-currents (I_{on}) of ~60 nA).[MS3,MS5] However, since the bottom-up synthesis commonly takes place on catalytic metallic surfaces, the integration of GNRs into such devices requires their transfer onto insulating substrates, which remains one of the bottlenecks in the development of GNR-based electronics. In response, the **Bokor** group developed a method for the transfer-free placement of GNRs on insulators, involving

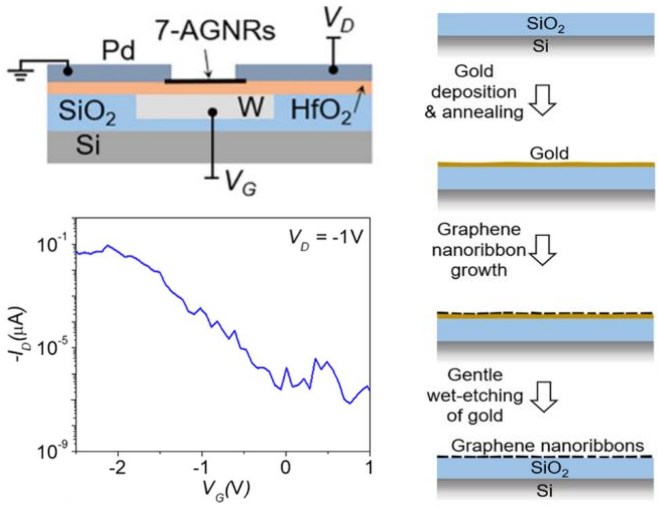


Figure 2. Left. Schematic representation (top) and I_D−V_G characteristics (bottom) of 7-AGNR FETs with Pd source−drain electrodes and local HfO_2 back gate. **Right.** Schematic of the transfer-free synthesis of GNRs on SiO_2/Si substrates. Typical AFM height images of a ~100 nm gold thin film deposited onto a SiO_2/Si substrate.

growth of GNRs on a gold film deposited onto an insulating layer followed by gentle wet etching of the gold, which leaves the nanoribbons to settle in place on the underlying insulating substrate (Figure 2, right).[MS5] Meanwhile, the team has also demonstrated transfer-free fabrication of ultrashort channel GNR FETs using this process. Importantly, this transfer-free process can scale up well to 12-inch wafers, which is extremely difficult for previous techniques.

B. Low-Temperature Semiconductor Processing

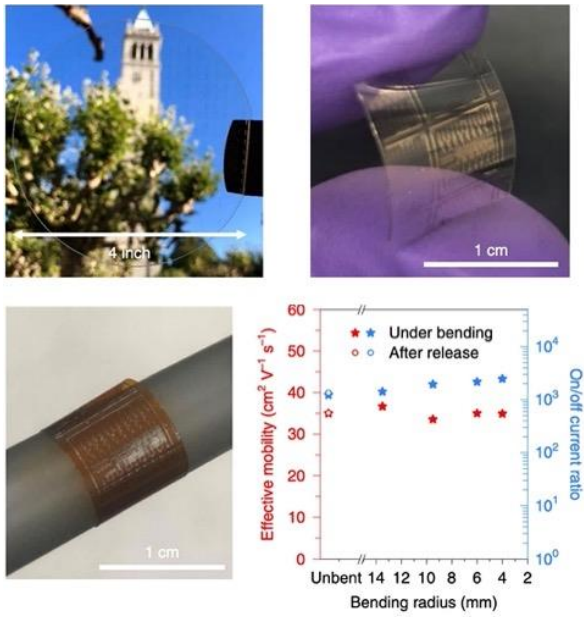


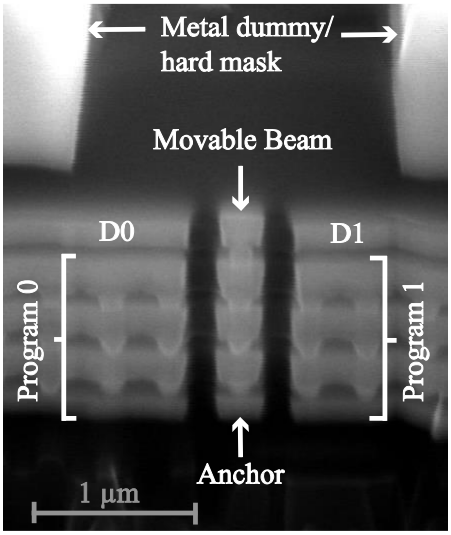
Figure 3. Photographs of Te FETs fabricated by evaporation with a substrate temperature of −80 C on 4-inch quartz wafer (**top, left**), on PET (**top, right**), and on Kapton (**bottom, left**) while bent (the thickness of the Kapton substrate is 50 μm). **Bottom, right.** Effective mobility and on/off current ratio of Te FET (8 nm) on Kapton substrate under different bending radii.

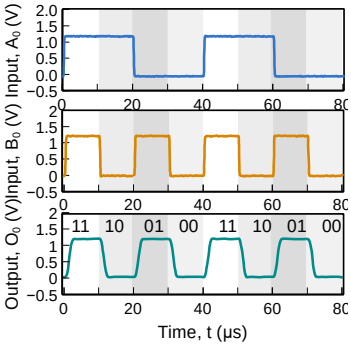
Processing of high-quality semiconductors at near-ambient temperatures has become increasingly important for both transparent/flexible electronics and monolithic 3D-CMOS architectures. While several solutions exist for n-type semiconductors, the **Javey** group recently reported a breakthrough for p-type semiconductors by successful thermal evaporation of tellurium thin films at cryogenic temperatures.[MS6] Using this approach, the team fabricated high-performance wafer-scale p-type field-effect transistors on various transparent and flexible substrates (Figure 3). The transistors have excellent properties, including high effective hole mobilities and ON/OFF current ratios, even under substantial bending. Moreover, various functional logic gates and 3D circuits were demonstrated by integrating multi-layered transistors on a single chip using sequential lithography, deposition and lift-off processes.

C. Non-Volatile Nano-Electromechanical (NEM) Switches

The **Liu** group has pioneered the use of non-volatile nano-electromechanical (NEM) switches (or relays) for energy efficient computing.[MS1,MS7] NEM switches use electrostatic force to mechanically actuate a movable structure to make or break physical contact between current-conducting electrodes. Importantly, when the electrodes are separated physically by an air gap, no current flows across the gap, resulting in zero OFF-state current. Hence NEM switches have abrupt ON/OFF switching characteristics, in addition to robust operation across a wide temperature range, down to cryogenic temperatures.[MS8] Moreover, NEM switches can be monolithically integrated with CMOS circuitry. This was demonstrated by the **Liu** group by implementation of non-volatile NEM switches using multiple metallic layers in the BEOL stack of a standard 65nm CMOS process, followed by a release etch after CMOS fabrication (Figure 4, left).[MS9,MS10] Low contact

resistance and reconfigurable circuit functionality was verified by operation of a vertical hybrid CMOS-NEM reconfigurable circuit. Program voltage is applied to either actuation electrode (Program0 or Program1) to electrostatically actuate the beam into contact with either D0 or D1 respectively. The contact adhesion force is designed to be higher than the spring restoring force to achieve non-volatile contacting states. A hybrid CMOS-NEM 2-input/1-output look-up table using 4x3 non-volatile NEM switch array is also demonstrated in Figure 4 (right).





Input		Output
A	B	O
0	0	0
0	1	1
1	0	0
1	1	1

Figure 4. Left. Cross-sectional SEM image of a vertical NEM switch fabricated in standard 65nm node, showing its five terminals in the as-fabricated state. **Right.** Input and output waveforms of a 2-input/1-output look-up table (LUT) based on non-volatile vertical NEM switches (top) and the corresponding truth table (bottom).

2.2.2 Current Projects

Graphene Nanoribbon-Based Millivolt Switches

(Prof. Jeffrey Bokor)

In collaboration with UC Berkeley synthetic chemist Prof. Felix Fischer, this project focusses on the synthesis of novel graphene nanoribbons (GNRs) and their integration into functioning field effect transistor (FET) devices. Recently, they demonstrated the excellent switching behavior of GNR-based FETs with ON/OFF ratios of ~10^5 and ON-currents (I_{on}) of ~60 nA.[MS3] Current work aims at upscaling GNR FET fabrication using a transfer-free placement of GNRs on insulators.[MS5] While the concept has been successfully demonstrated, the device performance was lower than with previous processes. The main focus now is to optimize this new transfer-free placement of GNRs process to increase both ON/OFF ratios and ON-currents. Since the transfer-free process can scale up well to 12-inch wafers, it is an important step toward large-scale integration of GNRs into electronic devices.

NEM Switches Monolithically Integrated with CMOS Circuitry

(Prof. Tsu-Jae King Liu)

Nanoelectromechanical (NEM) switches can be operated at ultralow voltages (<20 mV) and have abrupt ON/OFF switching characteristics, in addition to robust operation across a wide temperature

range. Taking advantage of ultra-scaled interconnect pitch in state-of-the-art CMOS technology, the team demonstrated that vertical non-volatile NEM switches can be implemented using multiple interconnect layers in the back-end-of-line (BEOL) stack of a standard 65nm CMOS process.[MS9,MS10] Such integrated systems have enormous potential for CMOS power gating, configuration of field-programmable gate arrays, non-volatile back-up storage of information in SRAM and CAM cells, and energy-efficient, fast and reconfigurable look-up tables. With support of BETR industry affiliate **SK Hynix**, the current project focuses on demonstration of BEOL NEM switches at extreme temperature conditions and on technology scaling to achieve programming voltage of NEM switches in the range compatible with standard I/O CMOS circuitry. A significant step in this direction has recently been achieved by demonstrating functional vertical non-volatile NEM switches and hybrid reconfigurable circuits in TMSC's 16nm FinFET CMOS process.

Monolithic 3D CMOS

(Prof. Ali Javey)

The Javey group has been exploring new materials and process schemes to enable synthesis of high electronic grade semiconductors at very low temperatures to enable monolithic 3D CMOS. That has been the primary challenge in achieving such architectures. They have developed a new growth mode, where single crystalline structures of III-V's can be grown on any substrate, including amorphous oxides at ~200 °C with high carrier mobility. Current work aims at exploring to advance the use of this platform for back-end electronics and 3D CMOS. In another approach, the group is looking at semiconductors, like Te that can self-crystalize at temperatures even below room temperature arising from their unique crystal structures.

2.2.3 Publications (Millivolt Switches – MS)

MS1. F. Chen, H. Kam, D. Markovic, T.J. King Liu, V. Stojanovic, and E. Alon, "Integrated Circuit Design with NEM Relays," *Proc. IEEE/ACM ICCAD*, pp. 750-757, Nov 2008.

MS2. S.B. Desai, S.R. Madhvapathy, A.B. Sachid, J.P. Llinas, Q. Wang, G.H. Ahn, G. Pitner, M.J. Kim, J. Bokor, C. Hu, H.-S.P. Wong, and A. Javey, "MoS2 Transistors with 1-Nanometer Gate Lengths," *Science*, vol. 354, pp. 99-102, Oct 2016.

MS3. J.P. Llinas *et al.*, "Short-Channel Field-Effect Transistors with 9-Atom and 13-Atom Wide Graphene Nanoribbons," *Nature Communications*, vol. 8, pp. 633, Sep 2017.

MS4. Y. Yang, R. Wilson, J. Gorchon, C.-H. Lambert, S. Salahuddin and J. Bokor, "Ultrafast Magnetization Reversal by Picosecond Electrical Pulses," *Science Advances*, vol. 3, pp. E1603117, Nov 2017.

MS5. Z. Mutlu, J.P. Llinas, P.H. Jacobse, I. Piskun, R. Blackwell, M.F. Crommie, F.R. Fischer, and J. Bokor, "Transfer-Free Synthesis of Atomically Precise Graphene Nanoribbons on Insulating Substrates," *ACS Nano*, vol. 15, pp. 2635-2642, Jan 2021.

MS6. C. Zhao, C. Tan, D.H. Lien, X. Song, M. Amani, M. Hettick, H.Y.Y. Nyein, Z. Yuan, L. Li, M.C. Scott, and A. Javey, "Evaporated Tellurium Thin Films for p-type Field-Effect Transistors and Circuits," *Nature Nanotechnology*, vol. 15, pp. 53-58, Jan 2020.

MS7. Z. A. Ye, S. Almeida, M. Rusch, A. Perlas, W. Zhang, U. Sikder, J. Jeon, V. Stojanović and T.-J. K. Liu, "Demonstration of Sub-50 mV Digital Integrated Circuits with Microelectromechnical Relays," *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec 2018.

MS8. X. Hu, S.F. Almeida, Z.A. Ye, and T.-J. King Liu, "Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications," *2019 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, pp. 34.2.1-34.2.4, Dec 2019.

2.3 Embedded Memory

*Research activities of the Embedded Memory Thrust have been supported in part by directed membership contributions of **SK Hynix**.*

Large data sets coupled with long network latency result in significant energy inefficiencies in data centers. Processors consume energy mostly in the idle state, waiting for the network to return a data query or maintaining availability to service a remote query into local memory. Disaggregation of processing and memory resources and optimization of the network fabric, enabled by new memory technologies and silicon photonics, can provide for dramatically improved energy efficiency of warehouse-scale computers. The BETR Center research groups of **Professors Jeffrey Bokor**, **Tsu-Jae King Liu**, **Ramamoorthy Ramesh**, **Sayeef Salahuddin**, and **Vladimir Stojanović** pursue the goal of high-density non-volatile memory that can be monolithically integrated with CMOS circuitry, such as nanometer-scale magnetic and ferroelectric devices, and nano-electro-mechanical switches (NEMS) implemented in a back-end-of-line process. This research involves fundamental scientific studies, to elucidate physical phenomena such as electric-field control of magnetization in multiferroic-ferromagnet heterostructures (for voltage-controlled operation of nanomagnetic memory devices), develop ultrafast (few picoseconds) magnetic devices, as well as the integration of memory+logic fabrication processes and characterization of three-dimensionally integrated circuit structures.[EM1-EM4]

2.3.1 Recent Achievements

A. Ultrafast Magnetic Switching

The **Bokor** and **Salahuddin** groups are developing current-driven, ultra-high speed magnetic elements for logic and memory with switching energies at the sub-femtojoule level.[EM4,EM5] Magnetic systems are attractive logic switches since their non-volatility can be used to reduce static power losses. However, the low speed of magnetic switching has severely limited device applications. The BETR research team demonstrated that ultrafast

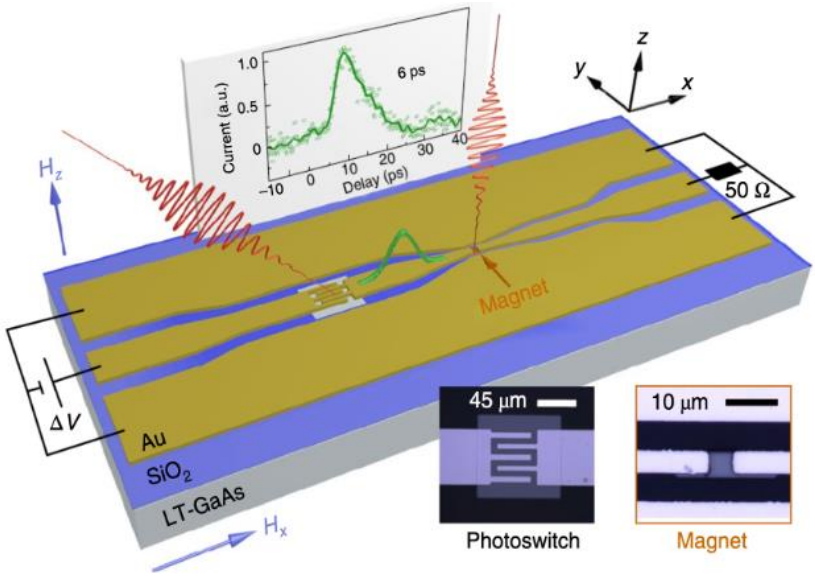


Figure 5. Ultrafast SOT switching set-up. Photogenerated ~6-ps-duration electrical pulses are guided and focused by a coplanar waveguide into the magnetic stack, resulting in ultrafast SOTs. The sampled picosecond current pulse is shown at the back of the figure. The solid green line is a guide to the eye.

switching of magnetic materials is possible by hot electrons that are excited via electrical pulses.[EM4] Moreover, a further breakthrough was recently achieved by the observation of spin-orbit torque (SOT) switching of a ferromagnet with picosecond electrical pulses.[EM5] In detail, it was discovered that photoconductive switches can be used to apply 6-ps-wide electrical pulses and deterministically switch the out-of-plane magnetization of a common thin cobalt film via spin–orbit torque (Figure 5). First results indicate that the magnetization switching consumes less than 50 pJ in micron-sized devices. Scaling down the device dimensions to 20 nm dimensions gives estimated switching energies of a few fJ, which is the current size of state-of-the-art magnetic memory devices.

B. NEM-Based Relays for Embedded Memory

The **Liu** and **Stojanović** groups have teamed up with support by BETR industry affiliate **SK Hynix** to explore system-based integrated circuit implementations in the so-called "edge computing" scenarios, where the sensory and computation functions are severely energy limited. For example, the team has investigated the use of NEM-based relays for applications as look-up tables (LUTs) and for embedded memory, including arrays of reconfigurable NEM-based interconnects for novel memory applications.[EM3] For this, vertically oriented relays were designed and fabricated by a standard 65nm CMOS process, using the multiple interconnect layers in the back-end-of-line (BEOL) process (Figure 7).[EM6,EM7] NEM switches are thus monolithically integrated with CMOS circuitry by performing a release etch after CMOS fabrication process with relatively low thermal budget. An analysis of the performance of NEMS switch-based embedded memories to increase the capacity and lower the energy-consumption per node is shown in Figure 7. The results demonstrate that with proper process node scaling, the NEMory can achieve very competitive metrics compared to CMOS-based memories and ReRAM.

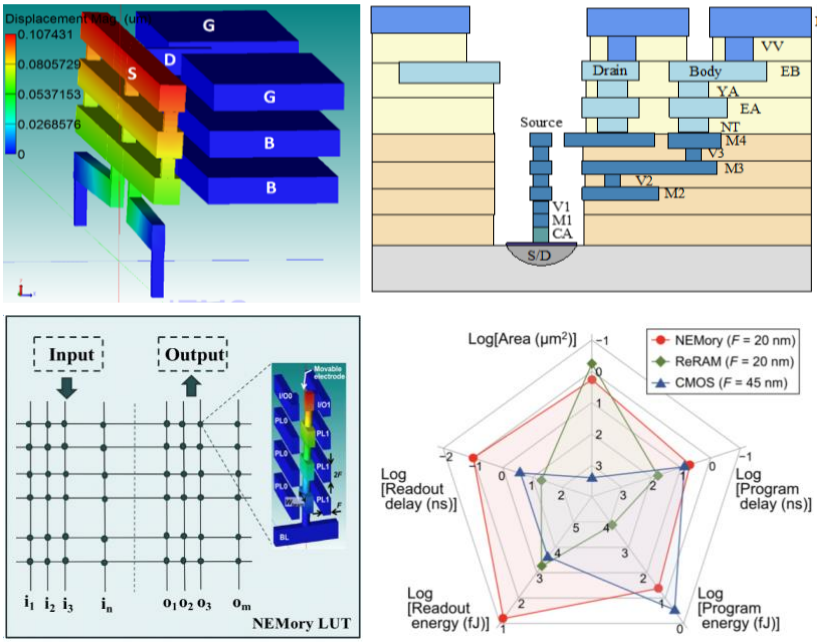


Figure 7. Top. NEM switches fabricated using multiple layers in a standard BEOL process in 65nm CMOS technology showing simulated structure of a vertically oriented body-biased relay (left) and schematic cross-section after sacrificial oxide etch (right). **Bottom.** NEMory performance comparison with ReRAM and CMOS.

C. Magnetoelectric Spin-Orbit (MESO) Logic

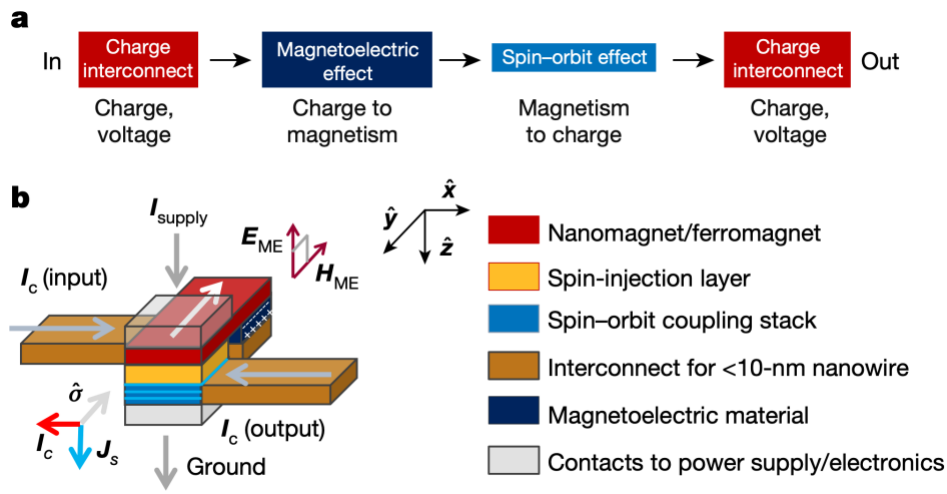


Figure 8. a) MESO logic transduction for a cascadable charge-input and charge-output logic device. **b)** MESO device comprising a spin-injection layer for spin injection from the ferromagnet to the topological material, an interconnect made of a conductive material, and contacts to the power supply and ground.

The **Ramesh** group is exploring pathways to drastically reduce the voltage requirement for electric field switching of multiferroics. Together with colleagues from **Intel**, the team developed a new logic computing concept based on a magnetoelectric spin–orbit (MESO) device with magnetoelectric switching nodes and spin–orbit-effect readout (Figure 8).[EM8] The ultimate goal is to switch magnets purely with a voltage of just 100 mV, or below. When successful, this will represent a 35-fold reduction in voltage amplitude compared to state of the art and a corresponding 1000-fold reduction in switching energy. This will also represent a paradigm shift in that no current will be necessary for switching magnetization.

2.3.2 Current Projects

Enabling MESO at 100 mV and Beyond

(Prof. Ramamoorthy Ramesh)

This project explores pathways to reduce electric field switching of multiferroics down to 100 mV using a new logic computing concept based on a magnetoelectric spin–orbit (MESO) device.[EM8] The project addresses the following challenges:

1. Is it possible to switch magnets purely with a voltage of just 100 mV? When successful, this will represent a 35X reduction in voltage amplitude compared to state of the art and a corresponding 1000X reduction in switching energy. This will also represent a paradigm shift where no current will be necessary to switch magnetization.
2. Is it possible to convert the state of a magnet into a voltage signal of the order of 100 mV? If successful, this will be 1000X improvement in the signal strength over the state of the art.
3. Is it possible to switch a magnetic order at 10s of picoseconds or less either with voltage or current? Note that this speed is ~10X faster than the state of the art and will bring

spintronic devices such as memory elements at the same level as the fastest electronic memory devices with the added advantage of non-volatility and infinite endurance.

To achieve these goals, the team will pursue three approaches: (i) chemically dope $BiFeO_3$ with La and Sm to reduce its coercive voltage; (ii) reduce the thickness of $BiFeO_3$ to thicknesses as small as 10 nm, while retaining the ferroelectric/antiferromagnetic properties; (iii) explore oxide ferromagnets as the top contact.

On-Chip Ultrafast Magnetic Switching

(Profs. Jeffrey Bokor, Sayeef Salahuddin, Vladimir Stojanović)

This project builds on the recent breakthrough of ultrafast spin-orbit torque (SOT) switching of a ferromagnet with picosecond electrical pulses.[EM5] Currently, the team is exploring on-chip ultrafast magnetic switching and readout triggered by electrical pulses generated directly by CMOS circuits. Conventional CMOS scaling is projected to reach transistor speeds in the range of a few picoseconds, so such electrical pulses will be available on-chip. To take advantage of this technology, the team works on integrating magnetic device structures on advanced CMOS chips. Two challenges have to be overcome toward this goal: (1) Integration of an electrical readout into the circuit structure, and (2) reduction of both the switching energy and current to be compatible with CMOS technology. In fact, calculations revealed that energies and currents for the electrical switching of magnets could be as low as ~3.5 fJ and ~10's of μA, respectively, for a $(20\ nm)^3$ cell size.

In-Memory and Normally-Off Computing Using Magnetic Nonvolatile Devices

(Profs. Jeffrey Bokor, Sayeef Salahuddin, Vladimir Stojanović)

This project focuses on the fabrication, design, and integration of in-memory and normally-off computing using magnetic nonvolatile devices with the goal of integrating three-terminal spin-Hall memory devices with a CMOS latch. The basic idea has been to reduce power by turning off large portions of the computer that are not in use. By using non-volatile memory, the shut-down part of the computer can readily be restored to its original state, once it is needed, without needing to write to or read from external storage. By distributing the memory over the circuit (memory-in-logic), additional power savings due to reduced interconnect length can be expected. Several spin-based devices added to SRAM circuits were evaluated and analysis across a number of various benchmarks promises 35 percent energy savings with this type of memory.

2.3.3 Publications (Embedded Memory – EM)

EM1. E. A. Tremsina, N. Roschewsky, and S. Salahuddin, "Micromagnetic Analysis and Optimization of Spin-Orbit Torque Switching Processes in Synthetic Antiferromagnets," *Journal of Applied Physics*, vol. 126, pp. 163905, Oct 2019.

EM2. N. Roschewsky, E. Walker, P. Gowtham, S. Muschinske, F. Hellman, S. Bank, and S. Salahuddin, "Spin-Orbit Torque and Nernst Effect in Bi-Sb/Co Heterostructures," *Physical Review B*, vol. 99, pp. 195103-195108, May 2019.

EM3. K. Kato, V. Stojanović, and T.-J. K. Liu, "Embedded Nano-Electro-Mechanical Memory for Energy-Efficient Reconfigurable Logic," *IEEE Electron Device Letters*, vol. 37, pp. 1563–1565, Dec. 2016.

EM4. Y. Yang, R. Wilson, J. Gorchon, C.-H. Lambert, S. Salahuddin, and J. Bokor, "Ultrafast Magnetization Reversal by Picosecond Electrical Pulses," *Science Advances*, vol. 3, pp. E1603117, Nov 2017.

EM5. K. Jhuria, J. Hohlfeld, A. Pattabi, E. Martin, A. Y. Arriola Córdova, X. Shi, R. Lo Conte, S. Petit-Watelot, J. C. Rojas-Sanchez, G. Malinowski, S. Mangin, A. Lemaître, M. Hehn, J. Bokor, R. B. Wilson, and J. Gorchon, "Spin–Orbit Torque Switching of a Ferromagnet with Picosecond Electrical Pulses," *Nature Electronics*, vol. 3, pp. 680-686, Oct 2020.

EM6. U. Sikder, G. Usai, T.-T. Yen, K. Horace-Herron, L. Hutin, and T.-J.K. Liu, "Back-End-of-Line Nano-Electro-Mechanical Switches for Reconfigurable Interconnects," *IEEE Electron Device Letters*, vol. 41, pp. 625-628, April 2020.

EM7. U. Sikder, L.P. Tatum, T.-T. Yen, and T.-J.K. Liu, "Vertical NEM Switches in CMOS Back-End-of-Line: First Experimental Demonstration and Programming Scheme," *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, pp. 21.2.1-4, Mar 2021.

EM8. S. Manipatruni, D.E. Nikonov, C.-C. Lin, T.A. Gosavi, H. Liu, B. Prasad, Y.-L. Huang, E. Bonturim, R. Ramesh, and I.A. Young, "Scalable Energy-Efficient Magnetoelectric Spin-Orbit Logic," *Nature*, vol. 565, pp. 35-43, Jan 2019.

2.4 Flexible and Wearable Electronics

Wearable and flexible electronics is one of the main research areas in the BETR Center with the goal of developing a new manufacturing and deployment paradigm for wearable, interactive information devices, including displays, sensors, and logic devices. Research activities are guided by the recognition that electronic devices must be non-intrusive, easily deployed and inexpensive, to become a pervasive technology. Spearheaded by the research groups of **Prof. Ali Javey** and **Prof. Ana Arias**, wearable and flexible electronics research in the BETR Center entails the development of tools, processes and materials for roll-to-roll processing, layer transfer, high-resolution printing, thin-film development, and packaging.[FE1,FE2]

2.4.1 Recent Achievements

A. Wearable Electronics for Sweat Monitoring

The **Javey** group used its expertise in microfluidics to design and fabricate wearable electronic patches for continuous sweat monitoring at rest.[FE3] The microfluidic design was optimized to combat evaporation, enable selective monitoring of secretion rate, and reduce required sweat accumulation times. In fact, the group developed a wearable device for rapid uptake of nL min^{-1} cm^{-2} rates of thermoregulatory sweat at rest, enabling near-real-time sweat rate and composition analysis at rest (Figure 9). Along with sweat rate sensors, the team also integrated electrochemical sensors for pH, chloride ion, and levodopa monitoring. They demonstrate patch functionality for dynamic sweat analysis related to routine activities, stress events, hypoglycemia-induced sweating, and Parkinson's disease, thus enabling continuous, autonomous monitoring of body physiology at rest. More generally, the developed patch can be used to study correlations between sweat rates and composition, helping to better understand analyte secretion mechanisms and guide how measured concentrations should be interpreted. Recently, the group also presented wearable sweat sensors with convenient glove-based form factors for sweat sensing under routine and even sedentary activity, making sweat-based biomarker monitoring practical for daily life.[FE4]

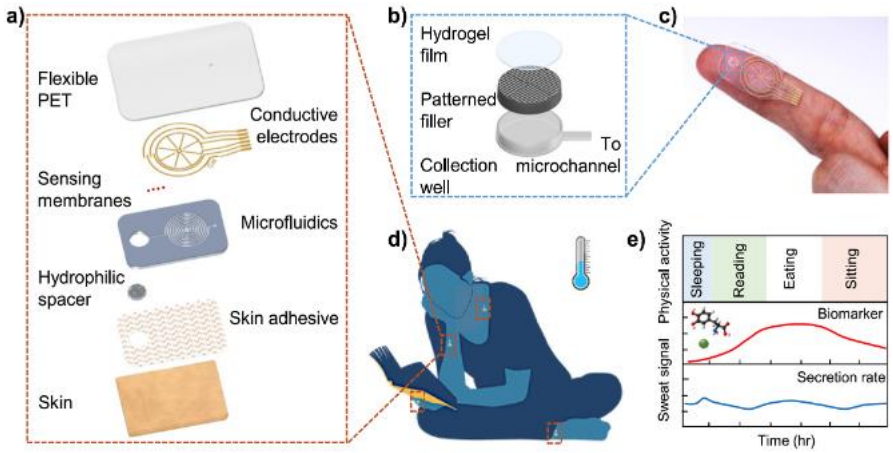


Figure 9. Schematic of the microfluidic sweat analysis patch containing multiple layers (a) and a hydrophilic filler to enhance sweat collection (b). An optical image of the sweat patch on a user's finger (c), or worn on various body locations (d), while continuously monitor both sweat secretion rate and compositions for long-term without external sweat stimulation (e).

B. Growth of Single-Crystal Semiconductors on Flexible Substrates

A flexible electronics breakthrough was recently reported by the **Javey** group by introducing a templated liquid-phase (TLP) crystal growth method, which enables direct growth of shape-controlled single-crystal III-Vs and group VI elements on amorphous substrates.[FE5,FE6] More importantly, growth of single-crystalline InP was demonstrated at substrate temperatures as low as 220 °C on low thermal budget substrates such as plastics and indium-tin-oxide (ITO)–coated glass (Figure 10).

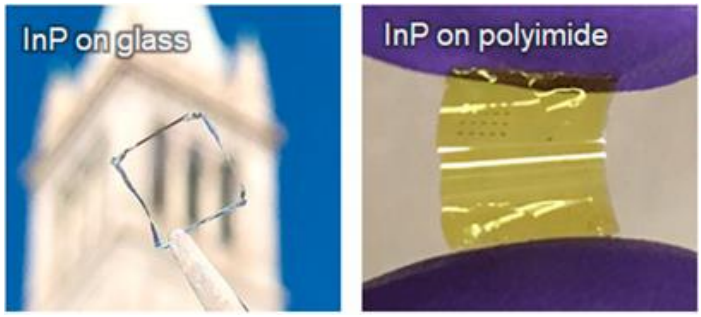


Figure 10. As-grown InP on ITO-coated glass (**left**), and peeled polyimide (**right**).

C. Electronic Skin by Mechanotransduction

The **Arias** group is developing various device fabrication methods based on roll-to-roll printing (screen and inkjet printing), blade coating, and organic binding techniques. For example, the team developed printed flexible composite Zn/MnO_2 batteries using organic gels as binder for the MnO_2 electrode.[FE7] Recently, the group also introduced fully flexible ambient light pulse oximeters from new organic photodiodes compatible with roll-to-roll printing techniques.[FE8] These new wearable devices can be combined with wireless data transmission capability. They demonstrated that these flexible devices accurately detect varying oxygen saturation levels in the body.

Inspired by the skin's sensory behavior, the **Arias** group developed a potentiometric mechanotransduction mechanism, which allows to encode mechanical stimuli into potential differences measured between two electrodes.[FE9] The devices were fabricated by an all-solution processing technique and exhibited ultralow-power consumption, high tunability, and a good capability to detect both static and low-frequency dynamic mechanical stimuli (Figure 11). Based on this potentiometric sensing mechanism, the group introduced two novel devices: (i) stretchable mechanical sensors with strain-independent performance and (ii)

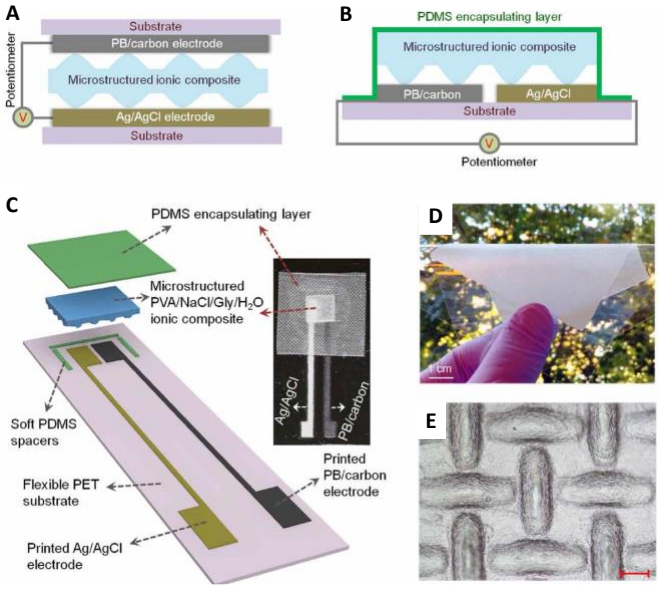


Figure 11. Schematic illustrations of the mechanotransducers with sandwich structure **(A)**, side-by-side electrode configuration **(B)**, and the all-solution processing approach **(C)**. Picture of a microstructured ionic composite film attached on a PET substrate **(D)**, and an optical micrograph showing the created microstructure on the surface of the ionic composite via a mesh-molding strategy **(E)**. Scale bar: 0.5 mm

single-electrode-mode e-skins with better pixel density and data acquisition speed compared with traditional dual-electrode-mode e-skins. This mechanotransduction mechanism has broad impact on robotics, prosthetics, and health care by providing a much-improved human-machine interface.

2.4.2 Current Projects

Wearable Sensors for Non-Invasive Continuous Monitoring of Biomarkers

(Prof. Ali Javey)

The goal of this proposal is to develop non-invasive sensors that can continuously monitor the concentrations of clinically relevant biomarkers in readily accessible bodily fluids, such as sweat.[FE1,FE3,FE4] The sensors will be used to perform medium to large scale population studies with vast time-series of data to generate personalized baselines indicative of the user's health. Over the last several years, the Javey group has developed a portfolio of wearable electrochemical sensors generally consisting of two main components that are interfaced together: (i) disposable sensor patch, and (ii) reusable electronics for signal condition, processing and transmission. They have developed roll-to-roll fabrication schemes for the sensor patches to enable a cost-effective method of mass producing the sensors through our collaboration with external partners, including VTT. The group has demonstrated small scale population studies to observe preliminary correlations for certain analytes, including pH, Cl^-, Na^+, vitamin C, nicotine, caffeine, and levodopa.

2.4.3 Publications (Flexible Electronics – FE)

FE1. Y. Yu, H.Y.Y. Nyein, W. Gao, and A. Javey, "Flexible Electrochemical Bioelectronics: The Rise of In Situ Bioanalysis," *Advanced Materials*, vol. 32, pp. 1902083, Apr 2020.

FE2. Y. Khan, A. Thielens, S. Muin, J. Ting, C. Baumbauer, and A.C. Arias, "A New Frontier of Printed Electronics: Flexible Hybrid Electronics," *Advanced Materials*, vol. 32, pp. 1905279, Apr 2020.

FE3. H.Y.Y. Nyein, M. Bariya, B. Tran, C.H. Ahn, B.J. Brown, W. Ji, N. Davis, and A. Javey, "A Wearable Patch for Continuous Analysis of Thermoregulatory Sweat at Rest," *Nature Communications*, vol. 12, pp. 1823, Mar 2021.

FE4. M. Bariya, L. Li, R. Ghattamaneni, C.H. Ahn, H.Y.Y. Nyein, L.-C. Tai, and A. Javey, "Glove-Based Sensors for Multimodal Monitoring of Natural Sweat," *Science Advances*, vol. 6, pp. eabb8308, Aug 2020.

FE5. M. Hettick, H. Li, D.H. Lien, M. Yeh, T.Y. Yang, M. Amani, N. Gupta, D.C. Chrzan, Y.-L. Chueh, and A. Javey, "Shape-Controlled Single-Crystal Growth of InP at Low Temperatures Down to 220 °C," *Proceedings of the National Academy of Sciences*, vol. 117, pp. 902-906, Jan 2020.

FE6. C. Zhao, C. Tan, D.H. Lien, X. Song, M. Amani, M. Hettick, H.Y.Y. Nyein, Z. Yuan, L. Li, M.C. Scott, and A. Javey, "Evaporated Tellurium Thin Films for p-type Field-Effect Transistors and Circuits," *Nature Nanotechnology*, vol. 15, pp. 53-58, Jan 2020.

FE7. A.M. Zamarayeva, A. Jegraj, A. Toor, V.I. Pister, C. Chang, A. Chou, J.W. Evans, and A.C. Arias, "Electrode Composite for Flexible Zinc–Manganese Dioxide Batteries through In Situ Polymerization of Polymer Hydrogel," *Energy Technology*, vol. 8, pp. 1901165, Mar 2020.

FE8. D. Han, Y. Khan, J. Ting, J. Zhu, C. Combe, A. Wadsworth, I. McCulloch, and A.C. Arias, "Pulse Oximetry Using Organic Optoelectronics under Ambient Light," *Advanced Materials Technologies*, vol. 5, pp. 1901122, May 2020.

FE9. X. Wu, M. Ahmed, Y. Khan, M.E. Payne, J. Zhu, C. Lu, J.W. Evans, and A.C. Arias, "A Potentiometric Mechanotransduction Mechanism for Novel Electronic Skins," *Science Advances*, vol. 6, pp. eaba1062, Jul 2020.

2.5 Hardware Accelerators for AI

The emergence of machine learning and other artificial intelligence applications has been accompanied by a growing need for new hardware architectures. The BETR Center research groups of **Professors Tsu-Jae King Liu**, **Sayeef Salahuddin**, **Vladimir Stojanović**, **Laura Waller**, and **Eli Yablonovitch** are investigating hardware accelerators specialized for large-scale matrix computations used in deep neural networks.[AI1-AI3] The BETR Center also develops new machines for solving difficult combinatorial optimization problems, such as those found in operations research, finance, and circuit design. The conventional von-Neumann computer is ill-suited for these applications in terms of latency and energy efficiency, due to its intrinsic architectural and algorithmic limitations, opening the door for alternative physical systems based on emerging technologies. BETR Center researchers investigate deep neural networks based on nanoelectromechanical relays and other novel switches, architecture-aware network pruning techniques, and analog machines that can solve NP-hard optimization problems without the need for the complexity of quantum bits.

2.5.1 Recent Achievements

A. Hardware-Accelerator Matched Compression Algorithms

A major research focus of the **Stojanović** group has been to develop hardware accelerator matched compression algorithms for deep neural networks (DNNs) to make them deployable on edge devices in real-time. For example, the team introduced the new MPDCompress algorithm based on matrix permutation decomposition. Through in-training application of random binary masks, a more efficient block-based implementation and compression was achieved.[AI1] Recently, the **Stojanović** group also introduced BagNet

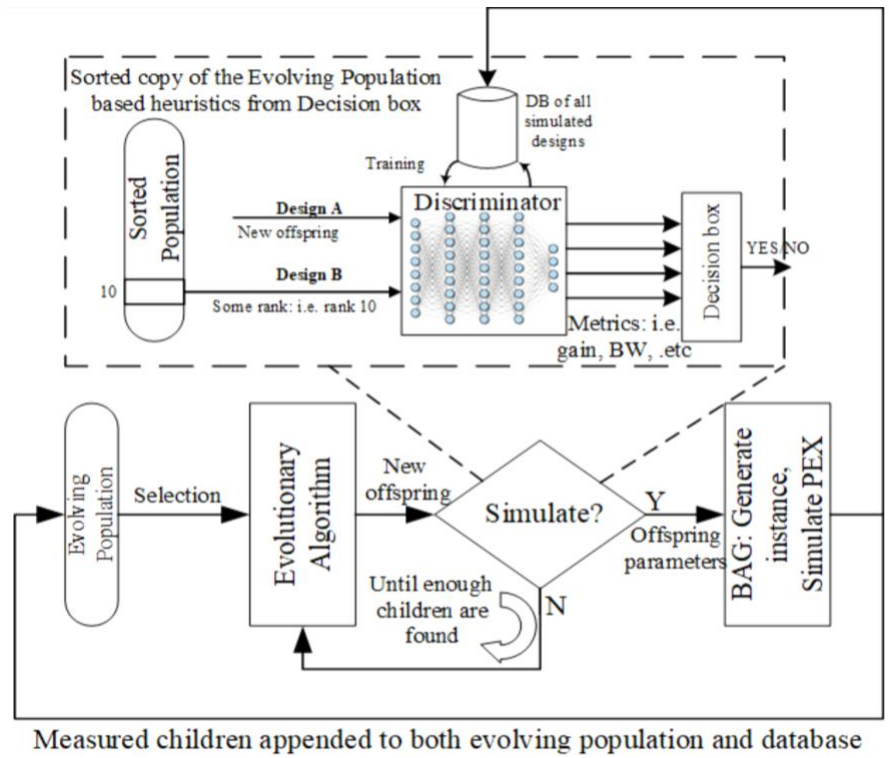


Figure 12. High-level architecture of the BagNet (Berkeley Analog Generator with Layout Optimizer) optimizer.

(Berkeley Analog Generator with Layout Optimizer) as a new optimization framework.[AI4] BagNet learns to reduce the number of simulations of evolutionary-based combinatorial optimizers using a DNN, which discriminates against generated samples, before running simulations (Figure 12). With this approach, the discriminator achieves at least two orders of magnitude improvement on sample efficiency for several large circuit examples.

B. Physics-Based Digital Optimization

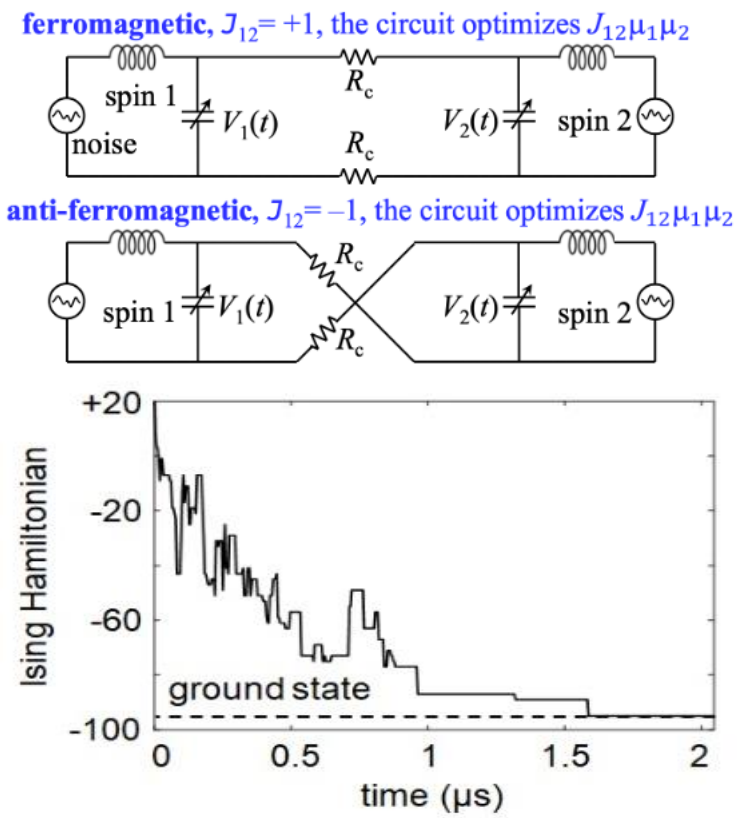


Figure 13. Top: Schematic of the LC oscillator system for a 2-spin problem. **Bottom:** Example of a 32-spin problem solved by the Yablonovitch system.

The **Yablonovitch** group investigates continuous-time analog machines for digital optimization, such as solving the computationally hard Ising Hamiltonian optimization problem, which describes the total interaction energy of any given network of coupled magnetic spins. The motivation for designing analog machines for the Ising problem is that there are physical principles in the domains of optics and electrical circuits, which can achieve orders-of-magnitude time speedups over digital algorithms while matching the quality of solutions obtained by them. In fact, physics itself, performs optimizations in the normal course of dynamical evolution and Nature provides a number of optimization principles. As an example, the team designed and analyzed an electrical LC oscillator-based Ising machine (Figure 13, top) based on Minimum Entropy Generation.[AI2] The **Yablonovitch** group also found that this system, as well as many previously developed systems, are in fact physical implementations of the well-known method of Lagrange multipliers in optimization theory.[AI5] In addition, optimization of a much larger class of merit functions beyond the Ising Hamiltonian can be performed by appropriate modifications of the electrical LC oscillator-based systems (Figure 13, bottom). This reinterpretation led the team to the conclusion that they possess now fast analog ways of performing Lagrange multiplier optimization with immediate application in a large number of areas involving optimization such as control systems, operations research and artificial intelligence.

C. Restricted Boltzmann Machine Neural Networks

The **Salahuddin** group successfully used the Restricted Boltzmann Machine (RBM) as a stochastic neural network capable of solving NP-Hard combinatorial optimization problems efficiently.[AI6] By exploiting the intrinsic parallelism present in the RBM architecture on a flexible Field Programmable Gate Array (FPGA) based accelerator, the team showed that this sampling framework is competitive with state-of-the-art computing machines based on novel physics. In agreement with the findings by the **Yablonovitch** group,[AI5] this work showed that there is no scaling advantage for the accelerators based on novel physics, indicating that classical hardware is sufficient for solving the computationally difficult problems. The RBM structure and sampling algorithm were demonstrated for an Ising model problem (Figure 14). The input graph for the Ising model type algorithm is fully connected, with no restrictions on the size or magnitude of the weight matrix (Figure 14A). The Ising model is then mapped to an RBM by making two copies of each graph node and edge and arranging them into a bipartite graph (Figure 14B). One copy is in the "visible" layer neurons and one in the "hidden" layer neurons, with no intra-layer edges. Each physical copy of the neuron is connected by a "coupling" parameter, *C*, which constrains the two copies to be the same value. Due to the lack of intra-layer connections, the layers can be sampled in parallel (Figure 14C). Each of the neurons in a layer is sampled in parallel and used to calculate the values of the opposite layer, creating a two-step sampling procedure. This sampling procedure proceeds until the output of the algorithm has reached the ground state, or until the algorithm output is of sufficient quality.

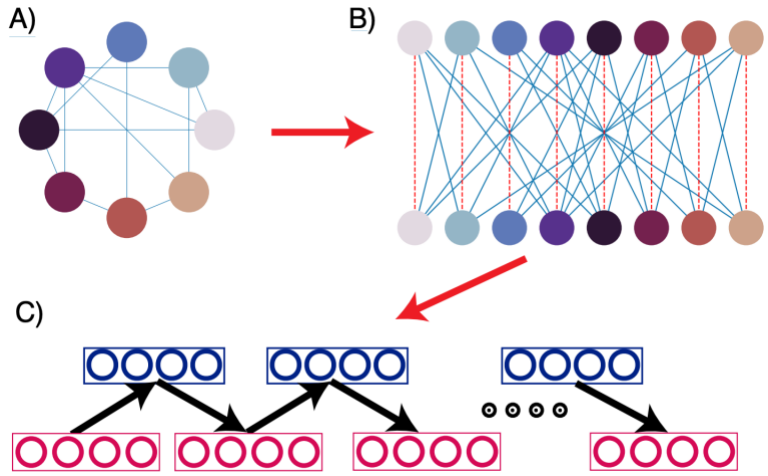


Figure 14. Demonstration of RBM structure and sampling algorithm. **A)** Structure of the input graph for an Ising model type algorithm. The graph is fully connected, with no restrictions on the size or magnitude of the weight matrix. **B)** Mapping of the Ising model to an RBM. **C)** Parallel sampling layers.

2.5.2 Current Projects

Photonic and Analog-Mixed Signal Generators

(Prof. Vladimir Stojanović)

The Stojanović groups is developing design automation tools for photonic and AMS design. Berkeley Photonic Generator has been developed to streamline the design and optimization of complex layout shapes needed for silicon-photonic designs for various applications. It plugs directly into the Berkeley Analog Generator framework enabling photonic-ams co-design. They

are also developing AI/ML based design automation methods on top of BAG to enable AMS circuits process porting and topology optimization.

Stochastic Neural Networks Based on Restricted Boltzmann Machines

(Prof. Sayeef Salahuddin)

The Salahudding group recently demonstrated that a restricted Boltzmann machine (RBM) can solve NP-Hard combinatorial optimization problems by exploiting the intrinsic parallelism present in the RBM architecture on a flexible Field Programmable Gate Array (FPGA) based accelerator.[6] The goal of this project is to show that further accelerator-level parallelization and scaling are possible through the use of multi-FPGA designs and communication, time division multiplexing, and more efficient pipeline stages. This will open the possibility of using parallel, stochastic computing to solve NP-Hard and NP-Complete problems with far reaching consequences in fields like logistics, scheduling, resource allocation, and many others.

Physics-Based Digital Optimization

(Prof. Eli Yablonovitch)

Optimization is vital to engineering, artificial intelligence, control theory and many areas of science. Mathematically, we usually employ steepest-descent, or other digital algorithms, however, physics itself, performs optimizations in the normal course of dynamical evolution. Nature provides us with the following optimization principles:

1. The Principle of Least Action
2. The Variational Principle of Quantum Mechanics
3. The Principle of Minimum Entropy Generation
4. The First Mode to Threshold Method
5. The Principle of Least Time
6. The Adiabatic Evolution Method
7. Quantum Annealing

In effect, physics can provide machines which solve digital optimization problems much faster than any digital computer. Of these physics-based principles, “Minimum Entropy Generation” in the form of bistable electrical or optical circuits is particularly adaptable toward offering digital Optimization.

Domain-Specific Accelerator Design

(Prof. Sophia Shao)

The Shao group is developing modular, high-performance, and reusable domain-specific accelerators for emerging applications like deep learning, robotics, and graphics. They aim to build an efficient and reusable infrastructure to enable designers to significantly improve the design productivity. The group is also interested in building machine-learning-driven design space exploration tools to quickly explore the large design space of accelerators.

(Recent publication: "Gemmini: Enabling Systematic Deep-Learning Architecture Evaluation via Full-Stack Integration", Design Automation Conference (DAC), December 2021. ***Preprint available upon request.****)*

Accelerator Integration

(Prof. Sophia Shao)

The Shao group is developing systematic methodologies and optimizations to enable efficient accelerator integration with the rest of System-on-Chip and/or System-in-Package. The goal is to holistically understand the system-level interactions across accelerators, general-purpose cores, and shared resources so that they can efficiently execute a wide range of applications in future-generation of SoCs and SiPs.
(Recent publication: "Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs", IEEE Micro Special Issue on Agile and Open-Source Hardware, July/August 2020. ***Preprint available upon request.****)*

Accelerator Programming Infrastructure

(Prof. Sophia Shao)

The Shao group is building high-productivity programming infrastructure to enable fast and efficient mapping of applications to domain-specific systems. In particular, they leverage the regularity in both applications and domain-specific systems and formulate the programming problems as a constrained-optimization problem. The group demonstrated that by leveraging advances in integer-linear programming and deep reinforcement learning, they can quickly find performant scheduling solutions without going through expensive, brute-force search.
(Recent publication: "CoSA: Scheduling by Constrained Optimization for Spatial Accelerators", to appear in the International Symposium on Computer Architecture (ISCA), June 2021.)

2.5.3 Publications (Artificial Intelligence – AI)

AI1. L. Supic, R. Naous, R. Sredojevic, A. Faust, and V. Stojanović, "MPDCompress - Matrix Permutation Decomposition Algorithm for Deep Neural Network Compression," *arXiv*:1805.12085, May 2018.

AI2. E. Yablonovitch, T. P. Xiao, and S. K. Vadlamani, "Classical Machines, for Solving the Toughest Problems in Computer Science," in *Frontiers in Optics + Laser Science APS/DLS*, OSA Technical Digest (Optical Society of America, 2019), paper JTu4A.114, Sep 2019.

AI3. M. Kellman, M. Lustig, L. Waller, "How to do Physics-based Learning," *arXiv*:2005.13531, May 2020.

AI4. K. Hakhamaneshi, N. Werblun, P. Abbeel, and V. Stojanovic, "BagNet: Berkeley Analog Generator with Layout Optimizer Boosted with Deep Neural Networks," *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA, 2019, pp. 1-8, Jan 2020.

AI5. S. K. Vadlamani, T. P. Xiao, and E. Yablonovitch, "Physics Successfully Implements Lagrange Multiplier Optimization," *Proceedings of the National Academy of Sciences*, vol. 117, no. 43, pp. 26639-26650, Oct 2020

AI6. S. Patel, L. Chen, P. Canoza, and S. Salahuddin, "Ising Model Optimization Problems on a FPGA Accelerated Restricted Boltzmann Machine," *arXiv*:2008.04436, Oct 2020.

2.6 System Integration

Future information and communication (ICT) applications set a broad context for research conducted in the BETR Center research groups of **Professors Jeffrey Bokor**, **Tsu-Jae King Liu**, **Sophia Shao**, and **Vladimir Stojanović**. While system integration research efforts in the BETR Center are complementary to other industry-sponsored centers such as the Berkeley Wireless Research Center (BWRC), collaborative projects with BWRC serve to bridge innovations in physical electronics together with innovations in IC design, for co-optimization of new solid-state device technologies and computer architectures.[SI1-SI4] Through device modeling and simulation of integrated systems, tradeoffs between energy efficiency and performance can be optimized for a wide range of applications.

2.6.1 Recent Achievements

A. Optically Sampled Analog-to-Digital-Converter (O-ADC)

As the silicon-photonics (SiPh) processes mature, high-performance optical blocks integrated close to CMOS can be leveraged to alleviate system-level performance bottlenecks. For example, the accuracy of conventional analog-to-digital-converters (ADCs) for high-frequency input signals is mainly limited by the sampling clock jitter. To address this issue, the **Stojanović** group developed an ADC that uses low-jitter (<26 fsrms) optical pulses to sample the input signal.[SI5] The team then realized a prototype two-channel ADC in a 3D integrated platform with 65nm CMOS and silicon-photonics connected using high-density through-oxide-vias (TOVs), representing the first SiPh O-ADC fully integrated on a single-chip. Figure 15 shows the architecture of an O-ADC. An MLL-based external optical pulse source generates pulses at wavelengths λ_1 to λ_N with a given pulse width, spacing, and repetition rate. An electro-optic modulator modulates the intensity of these pulses with the input signal. These pulses are then coupled into a SiPh chip where they are separated by the tunable double-ring bandpass filters matched to λ_1–λ_N. Thermal tuning circuits on the CMOS chip tune the filters to the desired wavelength. Photodetectors in each channel convert the optical pulses into current pulses that are amplified and

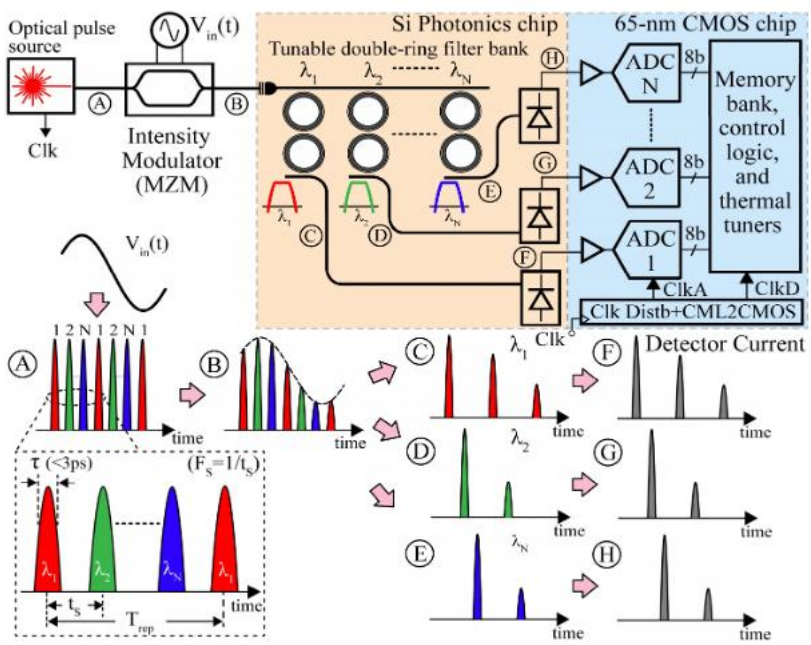
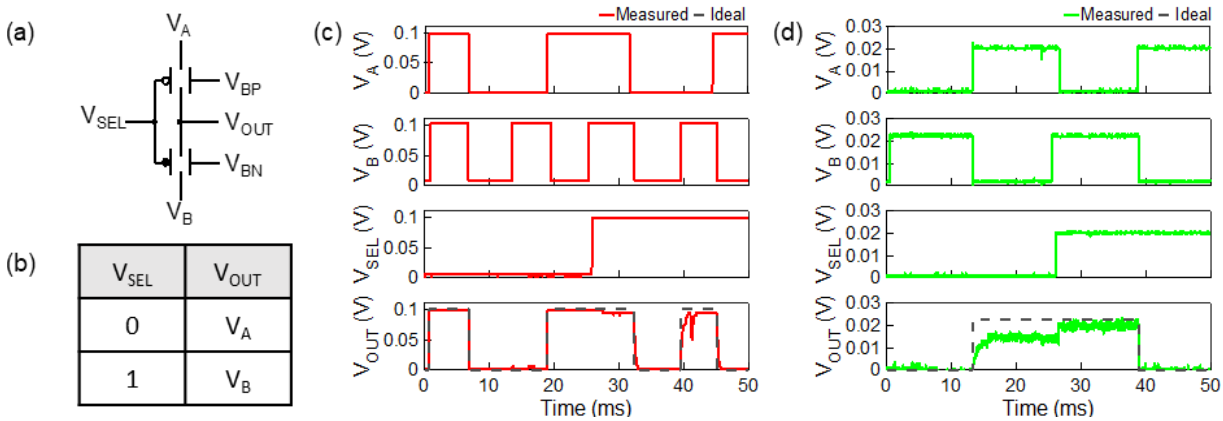


Figure 15. Architecture of an optically sampled analog-to-digital-converter (O-ADC).

digitized by the analog frontend (AFE) on the CMOS chip. The O-ADC presented here is fabricated in a 300mm CMOS foundry and achieves >5.5-bit resolution and input sampling bandwidth of 45 GHz.

B. Relay-Based Digital Integrated Circuits

In a collaborative project between the **Liu** and the **Stojanović** groups, reliable operation of relay-based digital integrated circuits (ICs) with 50 mV supply voltage was demonstrated.[SI3,SI6] No other digital IC device technology developed to date has even been projected to be able to operate at such low voltages at room temperature. Because a relay is much more functional than a transistor, various two-input logic functions (including NOT, AND, OR, and XOR) can be implemented with only two relays using pass-gate circuit topology, which minimizes the number of relays and the delay per digital function. Figure 16 shows a 2:1 multiplexer (MUX) implemented with only two relays; for comparison, a CMOS implementation requires at least four transistors.



V_{SEL}	V_{OUT}
0	V_A
1	V_B

Figure 16. Demonstration of ultra-low-voltage operation of a 2-to-1 multiplexer integrated circuit: (a) schematic circuit diagram and (b) truth table; measured voltage waveforms (c) at 300 K (V_{BP}=15.5 V, V_{BN}=-14.6 V) and (d) at 77 K (V_{BP}=17.07 V, V_{BN}=-14.71 V).

C. Single-Chip Optical Phased Array (OPA)

The **Stojanović** group developed an optical phased array (OPA) design based on a wafer-scale 3-D photonics/CMOS integration platform to resolve I/O and electronics density problems.[SI7] This research directly addresses the need for integrated OPAs to support 500-1000 elements in spite of stringent area/power/cost constraints in order to be a reliable solid-state alternative to mechanical beam scanners for automotive LiDAR. The team designed a compact single-chip OPA through wafer-scale 3-D integration of silicon photonics and CMOS, as shown in Figure 17. Flexible and ultra-dense connections with through-oxide vias (TOVs) resolve the I/O density issue. Moreover, low-voltage L-shaped phase shifters and compact, efficient switch-mode drivers, connected vertically using TOVs, remove wiring and placement overhead and achieve a large active array

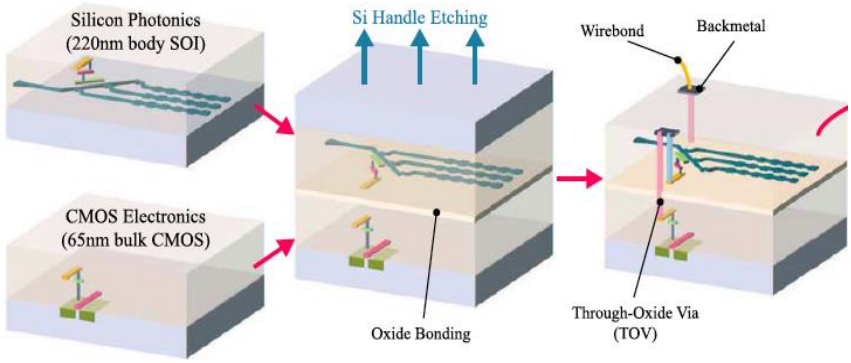


Figure 17. Overview of the 3-D heterogeneous integration platform used to construct the single-chip OPA.

aperture within a compact die. This OPA prototype achieves wide-range 2-D steering while consuming 20 mW/element average power. Furthermore, 3-D integration allows the photonics to be highly customized independent of electronics, opening up unlimited opportunities for integrated free-space system design.

2.6.2 Current Projects

SuperFabric

(Prof. Vladimir Stojanović)

SuperFabric looks at design of WDM photonic links that work together with a MEMS-based optical switch (high-radix 128-1024 with sub-us switching time) to aid in scale-out of compute clusters for AI training. The photonic links have fast (sub-100ns) electro-optic wavelength lock and burst-mode CDR and laser forwarding to mitigate switch insertion losses.

mm-Wave Photonic WDM Links for Radar Phase-Array and Massive-MIMO Systems

(Prof. Vladimir Stojanović)

The goal of this project is to design antenna-to-photons analog mm-wave photonic links that minimize the power consumption at the phase-array panel, by converting mm-wave signals from the antenna directly to the optical domain with a mm-wave LNA chain directly modulating ring modulators specialized for mm-wave modulation. The remoted central processing site receivers use coherent demodulation to avoid mm-wave mixers and simplify the mm-wave receiver front-ends.

Relay-Based Digital Integrated Circuits

(Prof. Tsu-Jae King Liu)

Nanoelectromechanical (NEM) relays can achieve immeasurably low off-state leakage and can be operated with much lower voltage swing than any transistor. These devices are therefore excellent candidates for emerging Internet of Things (IoT) applications. Current research aims to demonstrate reliable room-temperature operation of relay-based digital integrated circuits at 10 mV. Key scientific questions that will need to be answered along the way include: 1) What is the fundamental lower limit of operating voltage for mechanical computing? 2) What are key properties of the optimal contact material for milli-Volt mechanical computing? Furthermore,

reliable sub-25 mV switching operation of NEM relays was achieved at temperatures below 100 Kelvin.[SI6] Currently, operation of relays and integrated circuits at temperatures below 1 Kelvin are explored. The goal is to evaluate their compatibility with milli-Kelvin temperatures required for quantum computing.

Cryo-Photonic WDM Links

(Prof. Vladimir Stojanović)

This project aims to design the photonic links that connect superconducting cryo circuits to the outside environment. Superconducting circuits produce signals with 2-4mV amplitudes, which are then converted to optical signals via CMOS pre-amplifier integrated with specialized ring resonator modulators. The link architecture (Coherent Ultrafast Reflective Link - CURL) is a highly asymmetric link to minimize the thermal dissipation in the cryo environment.

Quantum Photonics in CMOS

(Prof. Vladimir Stojanović)

In this project, platform building blocks for the photonic quantum computing will be designed. One of the most complex blocks is the photon pair source that produces correlated photon pairs (through laser modulation and nonlinear filtering) that are used as qubits in linear mixing operations. The Stojanović group is also working on developing APDs in the same process for detection of the photon pairs for computation read-out.

2.6.3 Publications (System Integration – SI)

SI1. K. Settaluri, C. Lalau-Keraly, E. Yablonovitch, and V. Stojanović, "First Principles Optimization of Opto-Electronic Communication Links," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 5, pp. 1270-1283, May 2017.

SI2. F. Chen, H. Kam, D. Markovic, T.J. King Liu, V. Stojanovic, and E. Alon, "Integrated Circuit Design with NEM Relays," *Proc. IEEE/ACM ICCAD*, pp. 750-757, Nov 2008.

SI3. Z. A. Ye, S. Almeida, M. Rusch, A. Perlas, W. Zhang, U. Sikder, J. Jeon, V. Stojanović and T.-J. K. Liu, "Demonstration of Sub-50 mV Digital Integrated Circuits with Microelectromechnical Relays," *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec 2018.

SI4. A.H. Atabaki *et al.*, "Integrating Photonics with Silicon Nanoelectronics for the Next Generation of Systems on a Chip," *Nature*, vol. 556, pp. 349-354, Apr. 2018.

SI5. N. Mehta, Z. Su, E. Timurdogan, J. Notaros, R. Wilcox, C. Poulton, C. Baiocco, N. Fahrenkopf, S. Kruger, T. Ngai, Y. Timalsina, M. Watts, and V. Stojanović, "An Optically Sampled ADC in 3D Integrated Silicon-Photonics/65nm CMOS," *2020 IEEE Symposium on VLSI Technology*, Honolulu, HI, pp. 1-2, Dec 2020.

SI6. X. Hu, S.F. Almeida, Z.A. Ye, and T.-J. King Liu, "Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications," *2019 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, pp. 34.2.1-34.2.4, Dec 2019.

SI7. T. Kim, P. Bhargava, C.V. Poulton, J. Notaros, A. Yaacobi, E. Timurdogan, C. Baiocco, N. Fahrenkopf, S. Kruger, T. Ngai, Y. Timalsina, M.R. Watts, and V. Stojanović, "A Single-Chip Optical Phased Array in a Wafer-Scale Silicon Photonics/CMOS 3D-Integration Platform," *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 3061-3074, Nov. 2019

2.7 Computational Imaging

*Research activities of the Computational Imaging/Metrology Thrust have been supported in part by directed membership contributions of **Lam Research**.*

Computational imaging is an emerging field of metrology, involving the co-design of imaging system hardware and software for optimization across the entire pipeline from acquisition to reconstruction. The defining idea is that computers can replace bulky and expensive optics by solving computational inverse problems. With this approach, new, computational-imaging-based microscopes can be designed for 3D aberration and phase measurement. Computational imaging research in the BETR Center is led by **Professor Laura Waller**, and it is focused on designing imaging systems and algorithms jointly using simple hardware, which is easily adoptable and advanced image reconstruction algorithms based on large-scale optimization and learning. The **Waller** group is also exploring a new direction in computational imaging by not just reconstructing images from a given data set but encoding the information in the hardware and using data-driven approaches to optimize capture of the images and set up of the physical system in conjunction with image reconstruction.[CI1] Recent BETR Center computational imaging research has focused on a feasibility study for transferring optical phase measurements for inspection of large optical components in the supply chain of BETR Center industrial affiliate **Lam Research.** The team is also conducting fundamental research in the field of EUV lithography that could be applied to various semiconductor applications, including probing thin-film structures to sub-atomic length-scales,[CI2] measuring phase of EUV masks for lithographic imaging,[CI3] and investigating next-generation designs for EUV photomasks.[CI4]

2.7.1 Recent Achievements

A. Picometer Sensitivity Metrology for EUV Absorber Phase

EUV attenuated phase shift masks have attracted considerable interest due to their superior image quality for applications such as dense contact and pillar arrays. With this growing interest, it has become critical to model, measure, and monitor the relative intensity and phase of multilayer and absorber reflections. The **Waller** group developed a solution based on physical modeling of reflectometry data, which is capable of achieving single picometer phase precision by characterizing the phase of an EUV photomask via measurements of reflectivity from multilayer and absorber regions (Figure 18).[CI2] The group derived a 28-parameter physical model, which was used to extract the effective propagation distance for each reflection coefficient in both regions. They also found that the absorber reflectivity changes systematically from one measurement to the next, unlike the multilayer which displayed changes during storage, but not during exposure. This was attributed to hydrocarbon contamination. Although these changes amount to only a fraction of an atomic monolayer, it was possible to determine the average thickness across the beam-spot to sub-atomic precision. The measurement precision was estimated to be 3-4 pm in terms of the 13.5 nm wavelength.

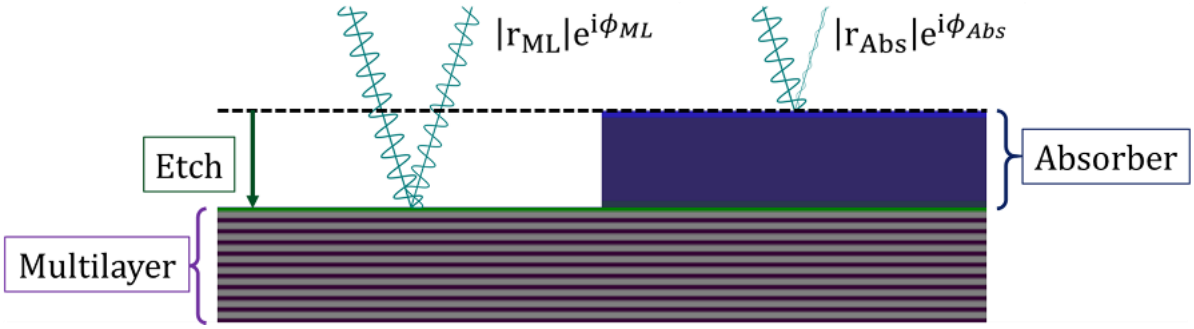


Figure 18. Schematic depiction of reflections from absorber and multilayer. Absorber layers from top to bottom are: TaON-Ta-Ru-(Si-MoSi-Mo-MoSi)x40. Multilayer uses same film-stack, with an additional etch depth parameter to replace etched layers with vacuum. An additional C layer is added on top of the absorber, representing hydrocarbon contamination.

B. EUV Microscope Characterization Using Photomask Surface Roughness

In a recent work, the **Waller** group developed a method for characterizing the aberrations of a full-field imaging system that does not require hardware modifications or the fabrication of test objects.[CI5] While the method was applied to the SHARP High-NA Actinic Reticle Review Project (an EUV microscope that operates near 13.5 nm wavelength, Figure 19), the team found that it is suitable for any full-field imaging system that has coherent, steerable illumination. To implement, speckle images of a suitable object at multiple angles of plane-wave illumination were acquired. Importantly, the object being imaged does not need to be precisely fabricated; it only needs to have a pseudo-random surface, weak phase and sufficient power-spectral density extending to the imaging system's resolution limit. For

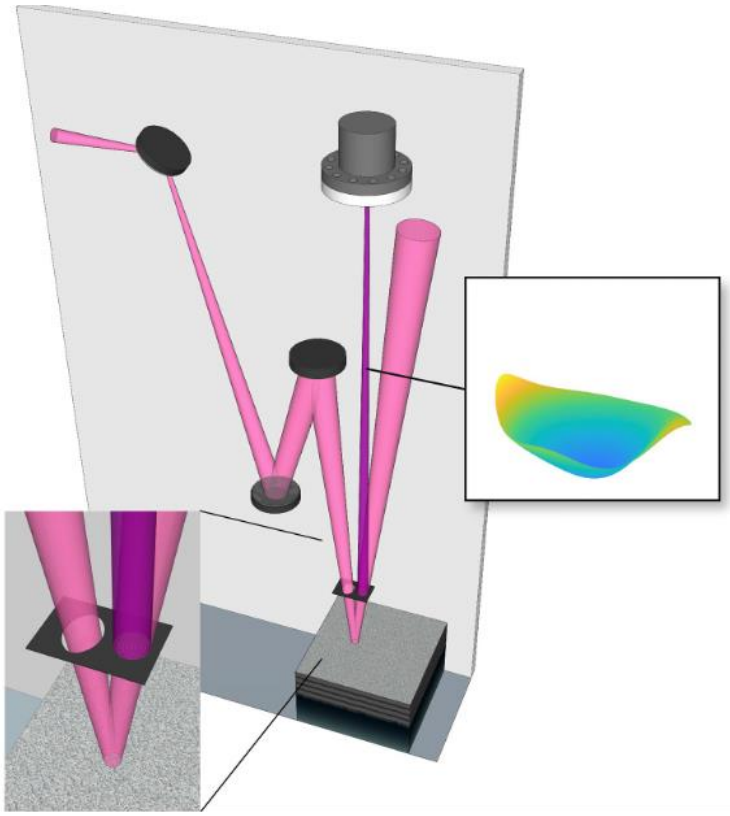


Figure 19. SHARP EUV microscope imaging configuration. A mirror conjugated with the object plane (which contains a blank EUV photomask) allows control over illumination angle. The objective lens (an off-axis Fresnel zone plate) images the beam scattered by the mask blank onto the sensor. The system suffers from field-dependent aberrations, primarily due to Petzval curvature.

example, the statistical uniformity of the inherent, atomic-scale roughness of readily available photomask blanks enables a self-calibrating computational procedure using images acquired under standard operation. Across a 30-µm field-of-view, a minimum aberration magnitude of smaller than $\lambda/21$ rms averaged over the center 5-µm area was demonstrated, with a measurement accuracy better than $\lambda/180$ rms. This method has several advantages over other approaches that entail imaging test objects. First, no special fabrication is required, as suitable objects can be found opportunistically. Second, unlike periodic objects, uncorrelated surface roughness provides isotropic sampling of frequency space. Third, no registration or alignment of the test object is required, as the statistics of the roughness should not change across the object. Finally, the method is data-efficient; in the current implementation, 10 speckle images were used to recover all field-varying aberrations of up to order 5.

2.7.2 Current Projects

Computational Microscopy for EUV Applications

(Prof. Laura Waller)

The Waller group is working on computational microscopy techniques applied to EUV and optical metrology. For example, they can use custom partially coherent illumination patterning and computational inverse problems, or phase masks in the pupil plane, to accurately recover the wavefront phase delays to a fraction of a wavelength, thus giving morphological measurements for masks and potentially wafer-level features. These methods offer resolution well beyond the diffraction limit imposed by the imaging system's numerical aperture, along with a large field-of-view for large-scale metrology applications.

2.7.3 Publications (Computational Imaging – CI)

CI1. L. Waller, "Computational Phase Microscopy," *Proc. SPIE, Biophotonics and Biomedical Microscopy*, vol. 11575, pp. 1157502, Oct 2020.

CI2. S. Sherwin, I. Cordova, R. Miyakawa, M. Benk, L. Waller, A. Neureuther, and P. Naulleau, "Picometer Sensitivity Metrology for EUV Absorber Phase," *Proc. SPIE, Extreme Ultraviolet Lithography 2020*, vol. 11517, pp. 1151707, Oct 2020

CI3. S. Sherwin, R. Miyakawa, M. Benk, L. Waller, A. Neureuther, and P. Naulleau, "Measuring EUV Mask 3D Effects with Hyperspectral Zernike Phase Contrast," *Proc. SPIE, Extreme Ultraviolet (EUV) Lithography XII*, vol. 11609, pp. 116090B, Mar 2021.

CI4. S. Sherwin, L. Waller, A. Neureuther, and P. Naulleau, "Advanced Multilayer Mirror Design to Mitigate EUV Shadowing," *Proc. SPIE, Extreme Ultraviolet (EUV) Lithography X*, vol. 10957, pp. 1095715, Mar 2019.

CI5. G. Gunjala, A. Wojdyla, S. Sherwin, A. Shanker, M. P. Benk, K. A. Goldberg, P. P. Naulleau, and L. Waller, "Extreme ultraviolet microscope characterization using photomask surface roughness," *Scientific Reports*, vol. 10, pp. 11673, Jul 2020.

2.8 Optical Interconnects and Integration

Silicon photonics technology is rapidly being adopted for high-speed communication between servers within data centers because optical signals can propagate faster and with better energy efficiency than voltage signals. Light also can be used to transmit data across a chip, through silicon microstructures which act as waveguides. However, significant improvements in the efficiency of miniature light emitters (lasers or light-emitting diodes, LEDs) and in the sensitivity of photodetectors are needed for optical interconnects to be more energy-efficient than electrical interconnects; the state of the art is hundreds of fJ/bit, orders of magnitude greater than the quantum limit of 20 aJ/bit. BETR Center researchers from the groups of **Professors Ali Javey**, **Vladimir Stojanović**, **Ming Wu**, and **Eli Yablonovitch** are addressing these needs by investigating the incorporation of optical antennas to enhance the spontaneous emission rate of LEDs, and by exploring novel approaches to alleviate tradeoffs between photodetector speed, capacitance, and optical absorption.[OI1-OI3] This research entails innovation of new optoelectronic device concepts, integration of advanced materials, and IC design breakthroughs to increase the communication bandwidth of silicon photonic chips.

2.8.1 Recent Achievements

A. Antenna-LED to Waveguide Optical Link

The **Wu** and **Yablonovitch** groups demonstrated an optical link by coupling the photoluminescence output of a high-efficiency III-V antenna-LED to an integrated optical waveguide.[OI4] The optical antenna-LED, invented in the Center for E^{3}S by **Wu** and **Yablonovitch**, is a fast and efficient nanoscale light source with spontaneous emission enhancements of more than 200 times under electrical excitation.[OI1] This is competitive with stimulated emission in lasers, but at drastically reduced power consumption. Using electromagnetic design techniques, the team engineered and optimized coupling efficiencies of antenna-LEDs to single mode optical waveguides. Epitaxial materials with different active regions were grown in collaboration with MIT researchers, as specified by modeling results from the BETR team (Figure 20, top). Figure 20 (middle) shows the structure after substrate removal. The dark field outline of the device is given at the bottom of Figure 20, with the overlaid photoluminescence map of the device. The average waveguide-coupling efficiency was estimated to be 85.9%. This remarkable result was obtained by calculating the ratio between the light coming from the grating to the total light collected from the structure and was confirmed by simulation methods.

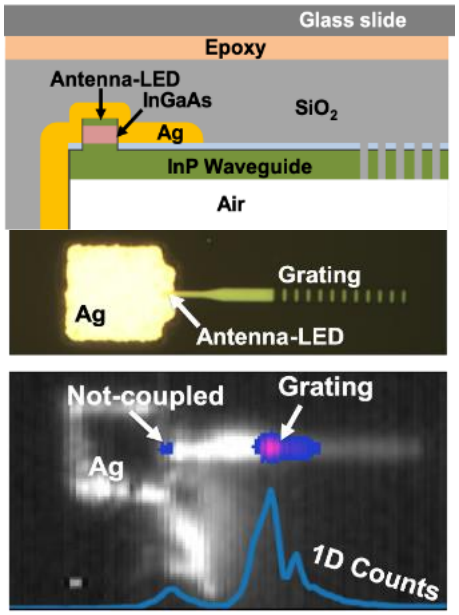


Figure 20. Top. Cross-sectional schematic of antenna-waveguide coupled structure. **Middle.** Optical micrograph of structure after substrate removal. **Bottom.** Dark field image of structure with 2D (heat map) and 1D counts overlaid.

B. IR-to-UV Generic Electroluminescence Device

The **Javey** group developed a unique light-emitting device that can excite electroluminescence from a wide variety of materials that emit in the long-wave infrared to ultraviolet wavelength range.[OI5] By using a porous carbon nanotube (CNT) network as the source contact and applying an a.c. gate voltage, band bending was generated, which can overcome carrier-injection barriers in transient mode operation and eliminates the need for emitter-specific charge-injection layers (Figure 21). The design allows the emitter layers to be deposited directly on top of the source contact, which lifts limitations on the processability of the light-emitting material. The team showed that an array of devices can be used to generate multiplexed electroluminescence emission, where each emitting material is deposited on one pixel of the array. They also demonstrated that the device can be used as a platform for electroluminescence spectroscopy and sensing. This approach creates opportunities for the development of light-emitting devices at extreme wavelengths, as well as the use of electroluminescence spectroscopy as a metrology and sensing technique for materials previously inaccessible to this type of analysis.

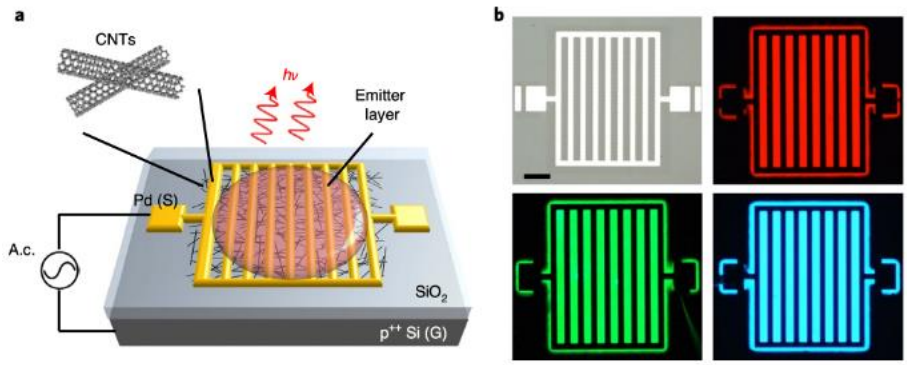


Figure 21. a) Device structure with an assembled CNT network on SiO2/Si and patterned source contact. The device operates by applying a.c. voltage between the metal grid on the CNT network (S) and Si backgate (G). **b)** Uniform EL can be excited with different emitters, including colloidal quantum dots and metal-organic complexes. Devices are measured with a 15-V, 100-kHz square wave. Scale bar, 0.1 mm.

C. 2D Random-Access Optical Beam Steering System

The **Wu** group developed a two-dimensional random-access optical beam steering system.[OI6] Such devices are the key components for many applications, including light detection and ranging (LiDAR) and free-space optical communications. Integrated beam steering devices with fast steering speed, low power consumption and large field-of-view (FoV) are highly demanded to address the drawbacks of their bulky mechanical counterparts. Optical phased arrays have been demons-

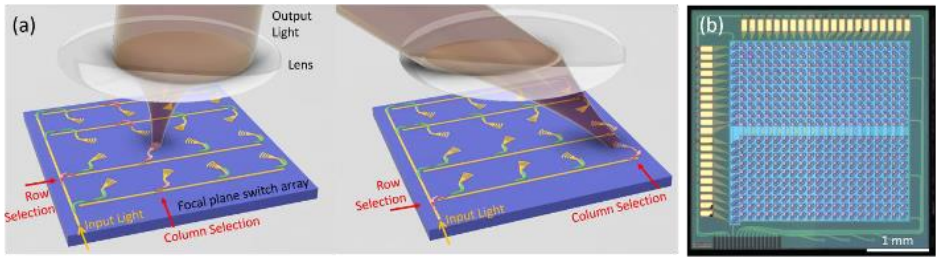


Figure 22. a) Schematic of the proposed beam steering system at two different steering angles. The actuated switches are in red color. For clarity, the MEMS actuators are not shown here. **b)** Microscope image of the fabricated 20×20 focal plane switch array on a 3.8×3.8 mm2 chip.

trated for 2D beam steering, however, they require precise control of thousands of phase shifting elements at the same time. The optical beam steering system introduced by the Wu group is much simpler and is composed of a 20×20 focal plane switch array integrated on a silicon photonics chip with microelectromechanical-system (MEMS) optical switches (Figure 22). The new device (based on MEMS-actuated silicon photonic switches demonstrated previously by the same team[7]) has a switch array with row-column addressing, random-access 2D beam steering with a FoV of 32°×32° and a beam divergence of 0.080°×0.086° with microsecond reconfiguration time. Moreover, the system can be extended to larger arrays by shrinking the pitch of the array and increasing the chip size.

2.8.2 Current Projects

Silicon Photonic Super-Switch

(Prof. Ming Wu)

The goal of this project is to develop large-scale silicon photonic switches (1000x1000) with fast response time (microsecond) and low optical loss (3dB fiber-to-fiber). This project has 3 tasks: Task 1 will develop scalable silicon photonic MEMS technology with super low loss. Task 2 will develop custom CMOS ASICs that will be directly flip-chip integrated on Si photonic switch for digital control. Task 3 will develop array fiber packaging technology with low insertion loss (< 0.5 dB). The team is currently in Phase 1 whose goal is to demonstrate 128x128 silicon photonic switch with integrated CMOS control and 8 dB fiber-to-fiber loss.

Development of Ultrafast LEDs

(Prof. Ali Javey)

The Javey group has identified a novel material based on molecular monolayers that exhibits near 100% photoluminescence quantum yield with a radiative lifetime of only 10 psec. The switching speed of a LED is limited by the carrier lifetime. For efficient/bright LEDs, a typical lifetime today is at best on the order of 10's of nsec. That limits how fast they can be switched. The team aims to use this new material class to make efficient LEDs with 10's of psec switching time. They have studied materials physics and now want to build devices to prove the concept.
(Recent publication: Zhao et al., "Strong optical response and light emission from a monolayer molecular crystal", Nature Communications, 10, 5589, 2019)

Efficient LEDs Based on Defect-Tolerant Materials

(Prof. Ali Javey)

Previously, the Javey group observed that for transition metal dichalcogenide (TMDC) monolayer semiconductors (e.g., MoS2, WS2, WSe2) there was a sharp drop in photoluminescence quantum yield (PLQY) at high exciton concentrations due to exciton-exciton annihilation (EEA), which is non-radiative. This was a major limitation for the use of monolayers in efficient practical devices. Recently (unpublished), they showed that EEA is resonantly amplified in TMDC monolayers by van Hove singularities (VHSs) present in their joint density of states. Logarithmic VHSs are a

hallmark of two-dimensional semiconductors. By applying small mechanical strain (~0.2%), the EEA process is shifted away from the VHS resonance and circumvent the enhanced nonradiative EEA that plagues the PLQY at high exciton densities, leading to near-unity PLQY at all exciton densities in 2D TMDC monolayers. Combined with counterdoping, this simple method suppresses all nonradiative recombination at all generation rates for both exfoliated and CVD-grown centimeter-scale TMDC monolayers. The group has studied materials physics and is now ready to build devices to prove the concept.

Packaging and Modeling of Si Photonic Switches and Wavelength-Selective Switches

(Prof. Ming Wu)

The goal of this project is to investigate silicon photonic switches and their applications in high performance computing systems and data centers. Specifically, the group will develop optical packaging for 4x4 and 16x16 switches demonstrated in the previous phase of this program. In addition, they will develop a model to predict the performance of the switch that integrates wavelength-division-multiplexing (WDM) components.

Compact Fourier Transform Infrared Spectrometer on Chip

(Prof. Ming Wu)

The goal of this project is to investigate and prototype chip-scale Fourier-Transform Infrared (FTIR) spectrometer enabled by low-loss silicon photonic micro-electro-mechanical-system (MEMS) switches and on-chip delay lines.

Variable Spectrum Optoelectronics

(Prof. Ali Javey)

Some 2D semiconductors exhibit a large band structure modulation by strain, larger than what is seen in classical systems. Furthermore, they can inherently tolerate larger strain values due to crystal structure. Taking advantage of these features, the Javey group has recently built actively variable spectrum LEDs and photodetectors for which a single device shows wavelength tunability from ~0.2 to 0.5 eV by applying a mechanical strain. It's effectively a MEMs device and by tuning the strain, the emission or absorption peak can be actively tuned from LWIR to mid-IR (unpublished, recently submitted). The group is exploring opportunities for various applications including spectroscopy.

Photonically-Remoted Endoscopic Ultrasound Array

(Prof. Vladimir Stojanović)

The Stojanović group is developing an ultrasound array readout beamforming system that consists of the low-power ring-resonator ultrasound sensor array chip (with thousands of sensors in an ultrasound probe integrated with ring thermal tuners) with a companion remoted receiver array chip. The ultrasound sensing capability of the ring resonator array opens the new applications beyond endoscopic ultrasound, such as photoacoustic imaging.

Photonic Label-Free Molecular Sensing

(Prof. Vladimir Stojanović)

The Stojanović group is using ring-resonators with integrated read-out circuits as molecular and viral nanoparticle sensors, developing the point-of-care and potentially implantable single-chip platforms for multi-analyte label-free sensing. Example application - multi-analyte (virus and antibody detection point-of-care testing for Covid-19).

2.8.3 Publications (Optical Interconnects – OI)

OI1. S. A. Fortuna, A. Taghizadeh, E. Yablonovitch, and M. C. Wu, "Toward 100 GHz Direct Modulation Rate of Antenna Coupled NanoLED," *IEEE Photonics Conference*, Jan 2016.

OI2. K. Settaluri, C. Lalau-Keraly, E. Yablonovitch, and V. Stojanović, "First Principles Optimization of Opto-Electronic Communication Links," IEEE Transactions on Circuits and Systems I: Regular Papers , vol.64, no.5, pp. 1270-1283, May 2017.

OI3. D.-H. Lien, M. Amani, S.B. Desai, G.H. Ahn, K. Han, J.-H. He, J.W. Ager, M.C. Wu, and A. Javey, "Large-Area and Bright Pulsed Electroluminescence in Monolayer Semiconductors," *Nature Communications*, vol. 9, pp. 1229, Mar 2018.

OI4. N. M. Andrade, Y. Kim, S. Hooten, E. Yablonovitch, J. Kim, M. C. Wu, "Efficient Coupling of an Optical Antenna-LED to a Single-Mode Waveguide," *IEEE Photonics Conference*, Oct 2020.

OI5. Y. Zhao, V. Wang, D.-H. Lien, and A. Javey, "A Generic Electroluminescent Device for Emission from Infrared to Ultraviolet Wavelengths," *Nature Electronics*, vol. 3, pp. 612-621, Oct 2020.

OI6. X. Zhang, K. Kwon, J. Henriksson, J. Luo, and M.C. Wu, "A 20×20 Focal Plane Switch Array for Optical Beam Steering," *2020 Conference on Lasers and Electro-Optics (CLEO)*, San Jose, CA, pp. 1-2, Sep 2020.

OI7. T.J. Seok, J. Luo, Z. Huang, K. Kwon, J. Henriksson, J. Jacobs, L. Ochikubo, R.S. Muller, and M.C. Wu, "Silicon Photonic Wavelength Cross-Connect with Integrated MEMS Switching," *APL Photonics*, vol. 4, pp. 100803, Oct 2019.

3. Knowledge Transfer

3.1 Overview

Knowledge transfer is at the heart of the BETR Center's mission of fostering groundbreaking discoveries and fertilizing new technologies. In the BETR Center, knowledge transfer is seen as a two-way street: Sharing the latest research outcomes of BETR with various stakeholders, while bringing new knowledge into the Center by engaging with its industry affiliate members and other key players in semiconductor technologies.

In fact, the BETR Center was established with the recognition that partnerships with leading semiconductor companies are a key factor in accelerating research, education and outreach endeavors. Since then, the Center has put significant efforts into sharing new knowledge with industry, academia and research labs. Interactions have taken place at various levels, including seminars/webinars by internal and external speakers, visits and customized briefings (online or in-person) for BETR Center industry affiliates, and biannual BETR Center workshops.

Additional knowledge transfer vehicles used by the BETR Center for sharing new discoveries with the wider research community are publications in scientific journals and conferences proceedings, as well as patents and invention disclosures. To that end, twice a year, the BETR Center shares a list of research publications (including copies of published papers) and patent applications with all industry affiliates. Moreover, if requested by an industry affiliate, technology licensing will be facilitated by introductions to the UC Berkeley Industry Alliances Office and Office of Technology Licensing.

Finally, the BETR Center recognizes that education itself is an important knowledge transfer element by preparing the Center's students and postdoctoral researchers to be the next-generation leaders in physical electronics and semiconductor technologies. The BETR Center facilitates interaction of Center students and postdocs with representatives of its industry affiliates through seminars/webinars, poster sessions at the biannual BETR Center Workshops, and targeted recruiting events (upon request by industry affiliates). Furthermore, the Center has been working with industry affiliates in identifying BETR Center students and postdocs for various internship positions.

In the following, detailed information about activities in the last year in BETR Center's four main knowledge transfer areas are provided:

- BETR Center Workshops
- Solid State Technology and Devices Seminars/Webinars
- Publications in Scientific Journals and Conference Proceedings
- Intellectual Property and Invention Disclosures

3.2 BETR Center Workshops

The workshops of the BETR Center are prime knowledge transfer opportunities, connecting faculty, postdocs and students of the Center with representatives of its industry affiliates and other invited companies from the semiconductor industry. These workshops are held twice annually. While, in the past, these workshops were held as in-person events, the last two workshops (spring and fall 2020) were held online due to COVID restrictions. Workshops feature oral presentations from BETR Center researchers, lightning talks and a poster session by the Center's students and postdocs, as well as an industry panel to discuss latest technology trends and challenges. In addition, all workshops include a one-hour closed session between the BETR Center leadership and members of the Technical Advisory Board (with representatives from all industry affiliates).

All workshop presentations are recorded and made available to industry affiliates on the BETR Center website (https://betr.berkeley.edu). Note that a BETR Center website account (with unique username/password) is needed to access the recordings. BETR Center website accounts may be requested by representatives of industry affiliates by email to betr@berkeley.edu.

Spring 2020 Workshop

The Spring 2020 Workshop of the BETR Center was held as a one-day online event on June 4, 2020 (see Appendix B for the full workshop agenda). The workshop was attended by 61 participants, including 18 BETR Center students and postdocs and 28 representatives from industry. It featured three talks by BETR Center co-directors and ten student/postdoc lightning talks, followed by a virtual poster session. Representatives of the following BETR Center industry affiliates participated in the closed session meeting of the Technical Advisory Board with BETR Center Leadership: **Applied Materials**, **Lam Research**, **TSMC**, and previous industry affiliate **Texas Instruments**.

Talks by BETR Center co-Directors

- **Ming Wu:** "Silicon Photonics for Sensing and Switching"
- **Ali Javey:** "Materials innovation for bright and fast LEDs"
- **Vladimir Stojanović:** "Integrated Electronics-Photonics for Sensing, Computing and Communication"

Lightning Talks and Posters by BETR Center Students and Postdocs

- **Christos-Georgio Adamopoulos** (Stojanović group): "A Fully Integrated Electronic-Photonic Platform for Label-Free Biosensing"
- **Zafer Mutlu** (Bokor group): "Transfer-Free Fabrication of Atomically Precise Graphene Nanoribbon Field-Effect Transistors"

- **Jason Hsu** (Salahuddin group): "Spin-Orbit Torque Generated by Amorphous FexSi1-x"
- **Xiaosheng Zhang** (Wu group): "A 20x20 Focal Plane Switch Array for Optical Beam Steering"
- **Jyotirmoy Chatterjee** (Bokor group): "KKY Exchange Coupling Mediated All-Optical Switching of a Ferromagnet"
- **Gautam Gunjala** (Waller group): "Error Analysis of Speckle Metrology for an EUV Imaging System"
- **Sri Krishna Vadlamani** (Yablonovitch group): "Physics Can Successfully Implement Lagrange Multiplier Optimization"
- **Mallika Bariya** (Javey group): "Wearable Sweat Sensors"
- **Stuart Sherwin** (Waller group): "Extending the Resolution of Extreme Ultraviolet Lithography with Attenuated Phase-Shift Masks"
- **Urmita Sikder** (Liu group): "Back-End-of-Line Nano-Electro-Mechanical Switches for Reconfigurable Interconnects"

Fall 2020 Workshop

In response to feedback received by the Technical Advisory Board at the 2020 Spring Workshop, the Fall 2020 Workshop of the BETR Center was extended to a two-day online event and was held on November 19 and 20, 2020 (see Appendix C for the full workshop agenda). The number of talks by BETR Center co-directors was increased to seven. In addition, 11 student/postdoc lightning talks were presented, followed by a virtual poster session. The Fall Workshop was attended by 63 participants, including 21 BETR Center students and postdocs and 26 representatives from industry. The closed session of the Technical Advisory Board with BETR Center leadership was attended by representatives of BETR Center industry affiliates **Applied Materials**, **Lam Research**, and **TSMC**.

Talks by BETR Center co-Directors

- **Eli Yablonovitch:** "Physics-Based Artificial Intelligence"
- **Tsu-Jae King Liu:** "Nano-Electro-Mechanical Switches for Future Computing Paradigms"
- **Jeffrey Bokor:** "New Developments in Ultrafast Spintronics"
- **Sayeef Salahuddin:** "Large Spin Orbit Torque in Amorphous FeSi"
- **Ana Claudia Arias:** "Power Sources for Flexible Electronic Devices"

- **Laura Waller:** "Computational Microscopy"
- **Sophia Shao:** "Hardware-Software Co-Design for Efficient Machine Learning Execution"

Lightning Talks and Posters by BETR Center Students and Postdocs

- **Zafer Mutlu** (Bokor group): "Bottom-up Graphene Nanoribbon Field-Effect Transistors with High Yield and Performance"
- **Jason Hsu** (Salahuddin group): "Enhanced spin-orbit torque in amorphous iron silicon"
- **Philip Jacobson** (Wu group): "Image Classification with Delay-Based Optoelectronic Reservoir Computing"
- **Debanjan Polley** (Bokor group): "A Simulation Study of Ultrafast Magnetization Reversal in Spin-Valve Structures"
- **Anju Toor** (Arias group): "Printed Miniaturized Batteries for Autonomous Microsystems"
- **Lars Tatum** (Liu group): "Device-Architecture Co-Optimization of Nonvolatile BEOL NEM Switch Arrays"
- **Hyungjin Kim** (Javey group): "Strain-Tunable Infrared Optoelectronics by Black Phosphorus"
- **Shehrin Sayed** (Salahuddin group): "Resonant enhancement of exchange coupling for voltage-controlled magnetic switching"
- **Stuart Sherwin** (Waller group): "Picometer Sensitive Metrology for EUV Absorber Phase"
- **Xiaodong Wu** (Arias group): "Bioinspired Electronic Skins for Thermosensation and Mechanosensation"
- **Sri Krishna Vadlamani** (Yablonovitch group): "Physics-based Machines for Energy-Efficient Optimization"

Industry Panel Discussion: "The New Normal After COVID"

- **Sayeef Salahuddin**, UC Berkeley (Moderator)
- **Philip Kraus**, Applied Materials (Panelist)
- **Nerissa Draeger**, Lam Research (Panelist)
- **Zia Karim**, Yield Engineering Systems (Panelist)
- **Dongik Suh**, SK Hynix (Panelist; pre-recorded)

3.3 Solid State Technology and Devices Seminar Series

Since September 2019 the BETR Center has been hosting the *Solid State Technology and Devices Seminar Series* of the UC Berkeley Electrical Engineering and Computer Science department. Solid State Technology and Devices seminars are usually held on Fridays (1:00-2:00 pm Pacific) by invited speakers who are experts from academia, national labs, and industry. While, in the past, all speakers were invited to visit UC Berkeley and seminars were held as in-person events (and simulcast to BETR Center industry affiliates by Webex videoconferencing), in the last year, all seminars had to be held online only due to COVID restrictions.

Seminars are usually recorded (with permission by the speaker) and made available to industry affiliates on the BETR Center website (https://betr.berkeley.edu). Note that a BETR Center website account (with unique username/password) is needed to access the seminar recordings. BETR Center website accounts may be requested by representatives of industry affiliates by email to betr@berkeley.edu.

Solid State Technology and Devices Seminars: July 2020 – May 2021

- **Sapan Agarwal**, Sandia National Laboratories, "A Survey of Emerging Beyond CMOS Devices and Architectures", July 23, 2020
- **Eric Yue Ma**, UC Berkeley, "Sensing Quantum Materials with New Electromagnetic Probes", September 18, 2020
- **Jeehwan Kim**, MIT, "Stackable Electronics Enabled by Freestanding 2D/3D Materials", September 25, 2020
- **Paolo Gargini**, IEEE, Chairman IRDS, "Use of the Roadmap (IRDS) Method to Overcome Industry Inflection Points", October 9, 2020
- **Ramamoorthy Ramesh**, UC Berkeley, "Electric Field Control of Magnetism", October 16, 2020
- **Zia Karim**, Yield Engieering Systems, "Low Thermal Budget Trends for Interconnect RDL Polyimides For 3D Advanced IC Backend Applications", October 23, 2020
- **Derya Baran**, KAUST, "Emerging Materials and Devices for Energy Harvesting Applications", November 6, 2020
- **Di Liang**, Hewlett Packard Labs, "Robust and Energy-Efficient VLSI Silicon Photonics for Communications and Computing", February 12, 2021
- **Chenming Hu**, UC Berkeley, "News and Future of Semiconductors", February 19, 2021
- **Vladimir Bulovic**, MIT, "Ubiquitous Active Surfaces", February 26, 2021

- **Gianlorenzo Masini**, Luxtera/Cisco, "Silicon Photonics: The Bumpy Road Toward Industrial Success", March 5, 2021
- **Jonathan Rivnay**, Northwestern University, "Organic Mixed Ionic/Electronic Conductors for Applications in Bioelectronics", March 12, 2021
- **Sara Mouradian**, UC Berkeley, "Engineering (Useful) Quantum Systems", March 19, 2021
- **Alp Sipahigil**, UC Berkeley, "Quantum Interconnects for Superconducting Quantum Processors", April 2, 2021
- **Huili Grace Xing**, Cornell University, "The Hunt for Mobile Holes Induced by Polarization in GaN", April 9, 2021
- **Michael Eggleston**, Nokia Bell Labs, "Integrated Optical Coherence Tomography: Continuous Physiological Monitoring and the Era of *Homo augmentus*", April 16, 2021
- **Mallika Bariya**, UC Berkeley, "Wearable Platforms for Sweat Sensing at Rest", April 23, 2021
- **Tomas Palacios**, MIT, "Electronics 5.0: New Materials and Devices for Edge Intelligence", April 30, 2021
- **Tahir Ghani**, Intel Corporation, "Innovations for Continuation of Moore's Law During Next 10 Years", May 7, 2021
- **Luqiao Liu**, MIT, "Magnonic Spintronics: Toward Spin Wave Based Information Processing", May 14, 2021

More details about the seminars/webinars, including abstract and speaker bio, can be found in Appendix A.

3.4 Publications (June 2020 – May 2021)

1. X. Zhang, H. Takeuchi, D. Connelly, M. Hytha, R.J. Mears, L.M. Rubin, and T.J. King Liu, "Tuning of Schottky barrier height using oxygen-inserted (OI) layers and fluorine implantation," *AIP Advances*, vol. 10, p. 065310, Jun 2020.
2. C. Sun, D. Jeong, M. Zhang, W. Bae, C. Zhang, P. Bhargava, D. Van Orden, S. Ardalan, C. Ramamurthy, E. Anderson, A. Katzin, H. Lu, S. Buchbinder, B. Beheshtian, A. Khilo, M. Rust, C. Li, F. Sedgwick, J. Fini, R. Meade, V. Stojanović, M. Wade, "TeraPHY: An O-band WDM Electro-optic Platform for Low Power, Terabit/s Optical I/O," *2020 IEEE Symposium on VLSI Technology*, Honolulu, HI, USA, pp. 1-2, doi: 10.1109/VLSITechnology18217.2020.9265012, Jun 2020.
3. N. Mehta, Z. Su, E. Timurdogan, J. Notaros, R. Wilcox, C. Poulton, C. Baiocco, N. Fahrenkopf, S. Kruger, T. Ngai, Y. Timalsina, M. Watts, V. Stojanović, "An Optically Sampled ADC in 3D Integrated Silicon-Photonics/65nm CMOS," *2020 IEEE Symposium on VLSI Technology*, Honolulu, HI, USA, Jun. 2020, pp. 1-2, doi: 10.1109/VLSITechnology18217.2020.9265101, Jun 2020.
4. A. J. Tan, M. Pešić, L. Larcher, Y.H. Liao, L. C. Wang, J.H. Bae, C. Hu, and S. Salahuddin, "Hot Electrons as the Dominant Source of Degradation for Sub-5nm HZO FeFETs," in *2020 IEEE Symposium on VLSI Technology*, pp. 1-2, doi: 10.1109/VLSITechnology18217.2020.9265067, Jun 2020.
5. Y.L. Huang, D. Nikonov, C. Addiego, R. V. Chopdekar, B. Prasad, L. Zhang, J. Chatterjee, H.J. Liu, A. Farhan, Y.H. Chu, M. Yang, M. Ramesh, Z. Q. Qiu, B. D. Huey, C. C. Lin, T. Gosavi, J. Íñiguez, J. Bokor, X. Pan, I. Young, L. W. Martin, and R. Ramesh, "Manipulating magnetoelectric energy landscape in multiferroics," *Nature Communications*, vol. 11, p. 2836, Jun 2020.
6. H. Pinkard, N. Stuurman, and L. Waller, "Pycro-manager: open-source software for integrated microscopy hardware control and image processing," *arXiv:2006.11330 [q-bio]*, Jun 2020.
7. R. Cao, M. Kellman, D. Ren, and L. Waller, "3D Differential Phase Contrast Microscopy with Axial Motion Deblurring," in *Imaging and Applied Optics Congress (2020)*, paper CF4C.2, Jun 2020.
8. G. Kuo, K. Monakhova, K. Yanny, R. Ng, and L. Waller, "Spatially-varying microscope calibration from unstructured sparse inputs," in *Imaging and Applied Optics Congress (2020)*, paper CF4C.4, Jun 2020.
9. E. Zhao, N. Deshler, K. Monakhova, and L. Waller, "Multi-sensor lensless imaging: synthetic large-format sensing with a disjoint sensor array," in *Imaging and Applied Optics Congress (2020)*, paper CF2C.6, Jun 2020.
10. K. Monakhova, K. Yanny, and L. Waller, "Snapshot hyperspectral imaging using a random phase mask and spectral filter array," in *Imaging and Applied Optics Congress (2020)*, paper JF2F.4, Jun 2020.

11. K. Yanny, N. Antipa, W. Liberti, S. Dehaeck, K. Monakhova, F. L. Liu, K. Shen, R. Ng, and L. Waller, "Compressed Sensing 3D Fluorescence Microscopy Using Optimized Phase Mask," in *Imaging and Applied Optics Congress (2020)*, paper CW4B.5, Jun 2020.

12. Y.H. Liao, D. Kwon, S. Cheema, A. J. Tan, M.Y. Kao, L.C. Wang, C. Hu, and S. Salahuddin, "Anomalous Subthreshold Behaviors in Negative Capacitance Transistors," *arXiv:2006.02594 [physics]*, Jun 2020.

13. C.H. Hsu, J. Karel, N. Roschewsky, S. Cheema, D. S. Bouma, S. Sayed, F. Hellman, and S. Salahuddin, "Spin-orbit torque generated by amorphous Fe x Si 1-x," *arXiv:2006.07786 [cond-mat]*, Jun 2020.

14. Z. Omair, S. Hooten, and E. Yablonovitch, "Optimized Optics for Highly Efficient Photovoltaic Devices," in *2020 47th IEEE Photovoltaic Specialists Conference (PVSC)*, pp. 1813-1815, Jun 2020.

15. E. Bostan, R. Heckel, M. Chen, M. Kellman, and L. Waller, "Deep phase decoder: self-calibrating phase microscopy with an untrained deep neural network," *Optica*, vol. 7, pp. 559-562, Jun 2020.

16. A. J. Tan, L. C. Wang, Y. H. Liao, J. H. Bae, C. Hu, and S. Salahuddin, "Reliability of Ferroelectric HfO2-based Memories: From MOS Capacitor to FeFET," 2020 Device Research Conference (DRC), Columbus, OH, USA, pp. 1-2, doi: 10.1109/DRC50226.2020.9135148, Jul 2020.

17. J. Zhu, D. Han, X. Wu, J. Ting, S. Du, and A. C. Arias, "Highly Flexible Transparent Micromesh Electrodes via Blade-Coated Polymer Networks for Organic Light-Emitting Diodes," *ACS Appl. Mater. Interfaces*, vol. 12, pp. 31687-31695, Jul 2020.

18. X. Wu, M. Ahmed, Y. Khan, M. E. Payne, J. Zhu, C. Lu, J. W. Evans, and A. C. Arias, "A potentiometric mechanotransduction mechanism for novel electronic skins," *Science Advances*, vol. 6, p. 1062, Jul 2020.

19. G. Gunjala, A. Wojdyla, S. Sherwin, A. Shanker, M. P. Benk, K. A. Goldberg, P. P. Naulleau, and L. Waller, "Extreme ultraviolet microscope characterization using photomask surface roughness," *Scientific Reports*, vol. 10, p. 11673, Jul 2020.

20. H. Liu, X. Yu, K. Wu, Y. Gao, S. Tongay, A. Javey, L. Chen, J. Hong, and J. Wu, "Extreme In-Plane Thermal Conductivity Anisotropy in Titanium Trisulfide Caused by Heat-Carrying Optical Phonons," *Nano Lett.*, vol. 20, pp. 5221-5227, Jul 2020.

21. S. S. Cheema, N. Shanker, C. H. Hsu, A. Dantar, J. Bae, D. Kwon, and S. Salahuddin, "One nanometer HfO2-based ferroelectric tunnel junctions on silicon," *arXiv:2007.06182 [cond-mat, physics:physics]*, Jul 2020.

22. M.Y. Kao, H. Agarwal, Y.H. Liao, S. Cheema, A. Dasgupta, P. Kushwaha, A. Tan, S. Salahuddin, and C. Hu, "Negative Capacitance Enables FinFET Scaling Beyond 3nm Node," *arXiv:2007.14448 [physics]*, Jul 2020.

23. A. Amid, D. Biancolin, A. Gonzalez, D. Grubb, S. Karandikar, H. Liew, A. Magyar, H. Mao, A. Ou, N. Pemberton, P. Rigge, C. Schmidt, J. Wright, J. Zhao, Y. S. Shao, K. Asanovic, and

B. Nikolic, "Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs," IEEE Micro, vol. 40, pp. 10-21, Jul/Aug 2020.

24. C. Tan, M. Amani, C. Zhao, M. Hettick, X. Song, D.H. Lien, H. Li, M. Yeh, V. R. Shreshta, K. B. Crozier, M. C. Scott, and A. Javey, "Evaporated Se x Te 1-x Thin Films with Tunable Bandgaps for Short-Wave Infrared Photodetectors," *Advanced Materials*, vol. 32, p. 2001329, Aug 2020.

25. E. Parsonnet, Y. L. Huang, T. Gosavi, A. Qualls, D. Nikonov, C.C. Lin. I. Young, J. Bokor, L. W. Martin, and R. Ramesh, "Toward Intrinsic Ferroelectric Switching in Multiferroic BiFeO3," *Phys. Rev. Lett.*, vol. 125, p. 067601, Aug 2020.

26. J. Gorchon, K. Jhuria, J. Hohlfeld, A. Pattabi, E. Martin, A. Y. Arriola Cordova, X. Shi, R. Lo Conte, S. Petit-Watelot, J.C. Rojas-Sanchez, G. Malinowski, S. Mangin, A. Lemaitre, M. Hehn, J. Bokor, and R. B. Wilson, "Picosecond spin orbit torque switching," in *Spintronics XIII*, vol. 11470, p. 114701I, Aug 2020.

27. A. C. Arias, "Vital signs monitoring enabled by flexible organic array of printed devices," in *Organic and Hybrid Field-Effect Transistors XIX*, vol. 11476, p. 1147602, Aug 2020.

28. D. Ren, C. Ophus, J. Zhou, H. DeVyldere, M. Whittaker, B. Gilbert, J. Banfield, M. Scott, J. Miao, and L. Waller, "3D Tomography for Multiple-scattering Samples Using Phase Contrast Electron Microscopy," *Microscopy and Microanalysis*, vol. 26, pp. 932-933, Aug 2020.

29. M. Bariya, L. Li, R. Ghattamaneni, C. H. Ahn, H. Y. Y. Nyein, L. C. Tai, and A. Javey, "Glove-based sensors for multimodal monitoring of natural sweat," *Science Advances*, vol. 6, p. eabb8308, Aug 2020.

30. L. Waller, "Physics-constrained computational imaging," in *Emerging Topics in Artificial Intelligence 2020*, vol. 11469, p. 114690M, Sep 2020.

31. S. Sayed, C.H. Hsu, N. Roschewsky, S.H. Yang, and S. Salahuddin, "Resonant Enhancement of Exchange Coupling for Voltage-Controlled Magnetic Switching," *Phys. Rev. Applied*, vol. 14, p. 034070, Sep 2020.

32. S. Z. Uddin, H. Kim, M. Lorenzon, M. Yeh, D.H. Lien, E. S. Barnard, H. Htoon, A. Weber-Bargioni, and A. Javey, "Neutral Exciton Diffusion in Monolayer MoS2," *ACS Nano*, vol. 14, pp. 13433-13440, Oct 2020.

33. A. M. Zamarayeva, N. A. D. Yamamoto, A. Toor, M. E. Payne, C. Woods, V. I. Pister, Y. Khan, J. W. Evans, and A. C. Arias, "Optimization of printed sensors to monitor sodium, ammonium, and lactate in sweat," *APL Materials*, vol. 8, p. 100905, Oct 2020.

34. C. L. Baumbauer, M. G. Anderson, J. Ting, A. Sreekumar, J. M. Rabaey, A. C. Arias, and Arno Thielens, "Printed, flexible, compact UHF-RFID sensor tags enabled by hybrid electronics," *Scientific Reports*, vol. 10, p. 16543, Oct 2020.

35. K. Yanny, N. Antipa, W. Liberti, S. Dehaeck, K. Monakhova, F. L. Lin, K. Shen, R. Ng, and L. Waller, "Miniscope3D: optimized single-shot miniature 3D fluorescence microscopy," *Light: Science & Applications*, vol. 9, p. 171, Oct 2020.

36. L. Waller, "Computational phase microscopy," in *Biophotonics and Biomedical Microscopy*, vol. 11575, p. 1157502, Oct 2020.

37. K. Monakhova, K. Yanny, K. Yanny, N. Aggarwal, and L. Waller, "Spectral DiffuserCam: lensless snapshot hyperspectral imaging with a spectral filter array," *Optica*, vol. 7, pp. 1298-1307, Oct 2020.

38. S. Sherwin, I. Cordova, R. Miyakawa, M. Benk, L. Waller, A. Neureuther, and P. Naulleau, "Picometer sensitivity metrology for EUV absorber phase," in *Extreme Ultraviolet Lithography 2020*, vol. 11517, p. 1151707, Oct 2020.

39. S. Patel, P. Canoza, and S. Salahuddin, "Logically Synthesized, Hardware-Accelerated, Restricted Boltzmann Machines for Combinatorial Optimization and Integer Factorization," *arXiv:2007.13489 [cs, stat]*, Oct 2020.

40. S. Patel, L. Chen, P. Canoza, and S. Salahuddin, "Ising Model Optimization Problems on a FPGA Accelerated Restricted Boltzmann Machine," *arXiv:2008.04436 [physics]*, Oct 2020.

41. M.Y. Kao, G. Pahwa, A. Dasgupta, S. Salahuddin, and C. Hu, "Analysis and Modeling of Polarization Gradient Effect on Negative Capacitance FET," *IEEE Transactions on Electron Devices*, vol. 67, pp. 4521-4525, Oct 2020.

42. P. Kushwaha, A. Dasgupta, M.Y. Kao, H. Agarwal, S. Salahuddin, and C. Hu, "Design Optimization Techniques in Nanosheet Transistor for RF Applications," *IEEE Transactions on Electron Devices*, vol. 67, pp. 4515-4520, Oct 2020.

43. T. Nan, Y. Lee, S. Zhuang, Z. Hu, J. D. Clarkson, X. Wang, C. Ko, H. Choe, Z. Chen, D. Budil, J. Wu, S. Salahuddin, J. Hu, R. Ramesh, and N. Sun, "Electric-field control of spin dynamics during magnetic phase transitions," *Science Advances*, vol. 6, p. eabd2613, Oct 2020.

44. S. K. Vadlamani, T. P. Xiao, and E. Yablonovitch, "Physics successfully implements Lagrange multiplier optimization," *Proceedings of the National Academy of Sciences*, vol. 117, pp. 26639-26650, Oct 2020.

45. Z. Omair, L. M. Pazos-Outon, M. A. Steiner, and E. Yablonovitch, "Accurate calibration of thermophotovoltaic efficiency," *PhotoniX*, vol. 1, p. 21, Oct 2020.

46. Y. Xue and L. Waller, "Computational hybrid imaging," *arXiv:2011.11574 [physics]*, Nov 2020.

47. X. Wu, J. Zhu, J. W. Evans, and A. C. Arias, "A Single-Mode, Self-Adapting, and Self-Powered Mechanoreceptor Based on a Potentiometric–Triboelectric Hybridized Sensing Mechanism for Resolving Complex Stimuli," *Advanced Materials*, vol. 32, p. 2005970, Nov 2020.

48. J. Hong, X. Li, N. Xu, H. Chen, S. Cabrini, S. Khizroev, J. Bokor, and L. You, "A Dual Magnetic Tunnel Junction-Based Neuromorphic Device," *Advanced Intelligent Systems*, vol. 2, p. 2000143, Nov 2020.

49. C. Zhao, L. Hurtado, and A. Javey, "Thermal stability for Te-based devices," *Appl. Phys. Lett.*, vol. 117, p. 192104, Nov 2020.

50. J.H. Bae, D. Kwon, J. Jeon, S. Cheema, A. J. Tan, C. Hu, and S. Salahuddin, "Highly Scaled, High Endurance, Ω-Gate, Nanowire Ferroelectric FET Memory Transistors," *IEEE Electron Device Letters*, vol. 41, pp. 1637-1640, Nov 2020.

51. C. Adamopoulos, A. Gharia, A. Niknejad, V. Stojanović, M. Anwar, "Microfluidic Packaging Integration with Electronic-Photonic Biosensors Using 3D Printed Transfer Molding," *Biosensors*, vol. 10, p. 177, Nov 2020.

52. K. Jhuria, J. Hohlfeld, A. Pattabi, E. Martin, A. Y. A. Cordova, X. Shi, R. Lo Conte, S. Petit-Watelot, J. C. Rojas-Sanchez, G. Malinowski, S. Mangin, A. Lemaitre, M. Hehn, J. Bokor, R. B. Wilson, and J. Gorchon, "Spin–orbit torque switching of a ferromagnet with picosecond electrical pulses," *Nature Electronics*, vol. 3, p. 680-686, Nov 2020.

53. J. Zhao, H. Y. Y. Nyein, L. Hou, Y. Lin, M. Bariya, C. H. Ahn, W. Ji, Z. Fan, and A. Javey, "A Wearable Nutrition Tracker," *Advanced Materials*, vol. 33, p. 2006444, Nov 2020.

54. H. Genc, S. Kim, A. Amid, A. Haj-Ali, V. Iyer, P. Prakash, J. Zhao, D. Grubb, H. Liew, H. Mao, A. Ou, C. Schmidt, S. Steffl, J. Wright, I. Stoica, J. Ragan-Kelley, K. Asanovic, B. Nikolic, and Y. S. Shao, "Gemmini: Enabling Systematic Deep-Learning Architecture Evaluation via Full-Stack Integration," *58th Design Automation Conference*, Dec 2021.

55. B. Osoba, S. F. Almeida, U. Sikder, Z. A. Ye, X. Hu, T. K. Etasu, and T. J. King Liu, "Study of MEM Relay Contact Design and Body-Bias Effects on on-State Resistance Stability," *Journal of Microelectromechanical Systems*, vol. 29, pp. 1531-1536, Dec 2020.

56. Y. Zhao, V. Wang, and A. Javey, "Molecular Materials with Short Radiative Lifetime for High-Speed Light-Emitting Devices," *Matter*, vol. 3, pp. 1832-1844, Dec 2020.

57. A. Moin, A. Zhou, A. Rahimi, A. Menon, S. Benatti, G. Alexandrov, S. Tamakloe, J. Ting, N. Yamamoto, Y. Khan, F. Burghardt, L. Benini, A. C. Arias, and J. M. Rabaey, "A wearable biosensing system with in-sensor adaptive machine learning for hand gesture recognition," *Nature Electronics*, vol. 4, pp. 54-63, Jan 2021.

58. A. Ceballos, A. Pattabi, A. El-Ghazaly, S. Ruta, C. P. Simon, R. F. L. Evans, T. Ostler, R. W. Chantrell, E. Kennedy, M. Scott, J. Bokor, and F. Hellman, "Role of element-specific damping in ultrafast, helicity-independent, all-optical switching dynamics in amorphous (Gd,Tb)Co thin films," *Physical Review B*, vol. 103, p. 024438, Jan 2021.

59. F. Ding, H.-Y. Wong, and T.-J. K. Liu, "Design optimization of sub-5 nm node nanosheet field effect transistors to minimize self-heating effects," *Journal of Vacuum Science & Technology B*, vol. 39, p. 013201, Jan 2021.

60. Z. Mutlu, J. P. Llinas, P. H. Jacobse, I. Piskun, R. Blackwell, M. F. Crommie, F. R. Fischer, and J. Bokor, "Transfer-Free Synthesis of Atomically Precise Graphene Nanoribbons on Insulating Substrates," *ACS Nano*, vol. 15, pp. 2635-2642, Jan 2021.

61. A. M. Zamarayeva, K. Gopalan, J. R. Corea, M. Z. Liu, K. Pang, M. Lustig, and A. C. Arias, "Custom, spray coated receive coils for magnetic resonance imaging," *Scientific Reports*, vol. 11, p. 2635, Jan 2021.

62. V. Wang, Y. Zhao, and A. Javey, "Performance Limits of an Alternating Current Electroluminescent Device," *Advanced Materials*, vol. 33, p. 2005635, Jan 2021.

63. S. Das, Z. Hong, V. A. Stoica, M. A. P. Goncalves, Y. T. Shao, E. Parsonnet, E. J. Marksz, S. Saremi, M. R. McCarter, A. Reynoso, C. J. Long, A. M. Hagerstrom, D. Meyers, V. Ravi, B. Prasad, H. Zhou, Z. Zhang, H. Wen, F. Gomez-Ortiz, P. Garcia-Fernandez, J. Bokor, J. Iniguez, J. W. Freeland, N. D. Orloff, J. Junquera, L. Q. Chen, S. Salahuddin, D. A. Muller, L. W. Martin, and R. Ramesh, "Local negative permittivity and topological phase transition in polar skyrmions," *Nature Materials*, vol. 20, p. 194-201, Feb 2021.

64. M. Goiriena-Goikoetxea, Z. Xiao, A. El-Ghazaly, C. V. Stan, J. Chatterjee, A. Ceballos, A. Pattabi, N. Tamura, R. Lo Conte, F. Hellman, R. Candler, and J. Bokor, "Influence of dislocations and twin walls in BaTiO3 on the voltage-controlled switching of perpendicular magnetization," *Phys. Rev. Materials*, vol. 5, p. 024401, Feb 2021.

65. Y. Wang, H. Pinkard, S. Zhou, L. Waller, and B. Huang, "Image denoising for fluorescence microscopy by self-supervised transfer learning," *bioRxiv*, 2021.02.01.429188, Feb 2021.

66. S. Sayed, S. Salahuddin, and E. Yablonovitch, "Spin–orbit torque rectifier for weak RF energy harvesting," *Appl. Phys. Lett.*, vol. 118, p. 052408, Feb 2021.

67. Z. Zhang, S. L. Hsu, V. A. Stoica, H. Paik, E. Parsonnet, A. Qualls, J. Wang, L. Xie, M. Kumari, S. Das, Z. Leng, M. McBriarty, R. Proksch, A. Gruverman, D. G. Schlom, L. Q. Chen, S. Salahuddin, L. W. Martin, and R. Ramesh, "Epitaxial Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ with Metallic Pyrochlore Oxide Electrodes.," *Advanced Materials*, vol. 33, p. 2006089, Feb 2021.

68. R. D. McCurdy, P. H. Jacobse, I. Piskun, G. C. Veber, D. J. Rizzo, R. Zuzak, Z. Mutlu, J. Bokor, M. F. Crommie, and F. R. Fischer, "Synergetic Bottom-Up Synthesis of Graphene Nanoribbons by Matrix-Assisted Direct Transfer," *J. Am. Chem. Soc.*, vol. 143, pp. 4174-4178, Mar 2021.

69. Z. A. Ye, S. F. Almeida, U. Sikder, X. Hu, T. K. Esatu, K. Le, J. Jeon, and T.-J. K. Liu, "Body-Biased Multiple-Gate Micro-Electro-Mechanical Relays," *IEEE Electron Device Letters*, vol. 42, pp. 402-405, Mar 2021.

70. F. Jakobs, T. A. Ostler, C.-H. Lambert, Y. Yang, S. Salahuddin, R. B. Wilson, J. Gorchon, J. Bokor, and U. Atxitia, "Unifying femtosecond and picosecond single-pulse magnetic switching in Gd-Fe-Co," *Physical Review B*, vol. 103, p. 104422, Mar 2021.

71. J. Liu, V. V. Laguta, K. Inzani, W. Huang, S. Das, R. Chatterjee, E. Sheridan, S. M. Griffin, A. Ardavan, and R. Ramesh, "Coherent electric field manipulation of Fe3+ spins in PbTiO3," *Science Advances*, vol. 7, p. eabf8103, Mar 2021.

72. H.Y.Y. Nyein, M. Bariya, B. Tran, C.H. Ahn, B.J. Brown, W. Ji, N. Davis, and A. Javey, "A Wearable Patch for Continuous Analysis of Thermoregulatory Sweat at Rest," *Nature Communications*, vol. 12, pp. 1823, Mar 2021.

73. Y.-H. Liao, D. Kwon, S. Cheema, N. Shanker, A. J. Tan, M.-Y. Kao. L.-C. Wang, C. Hu, and S. Salahuddin, "Electric Field-Induced Permittivity Enhancement in Negative-Capacitance FET," *IEEE Transactions on Electron Devices*, vol. 68, pp. 1346-1351, Mar 2021.

74. S. Sherwin, R. Miyakawa, M. Benk, L. Waller, A. Neureuther, and P. Naulleau, "Measuring EUV Mask 3D Effects with Hyperspectral Zernike Phase Contrast," *Proc. SPIE, Extreme Ultraviolet (EUV) Lithography XII*, vol. 11609, pp. 116090B, Mar 2021.

75. K. Monakhova, V. Tran, G. Kuo, and L. Waller, "Untrained networks for compressive lensless photography," *arXiv:2103.07609*, Mar 2021.

76. H. Pinkard, H. Baghdassarian, A. Mujal, E. Roberts, K. H. Hu, D. H. Friedman, I. Malenica, T. Shagam, A. Fries, K. Corbin, M. F. Krummel, and L. Waller, "Learned adaptive multiphoton illumination microscopy for large-scale immune response imaging," Nature Communications, vol. 12, p. 1916, Mar 2021.

77. S. Han, J. Beguelin, L. Ochikubo, J. Jacobs, T. J. Seok, K. Yu, N. Quack, C.-K. Kim, R. S. Muller, and M. C. Wu, "32 × 32 silicon photonic MEMS switch with gap-adjustable directional couplers fabricated in commercial CMOS foundry," *J. Optical Microsystems*, vol. 1, p. 024003, Mar 2021.

78. A. J. Tan, Y.-H. Liao, L.-C. Wang, J.-H. Bae, C. Hu, and S. Salahuddin, "Ferroelectric HfO_2 Memory Transistors with High- κ Interfacial Layer and Write Endurance Exceeding 10^{10} Cycles," *arXiv:2103.08806 [physics]*, Mar 2021.

79. M.-Y. Kao, S. Salahuddin, and C. Hu, "Negative Capacitance Enables GAA Scaling V_{DD} to 0.5V," *Solid-State Electronics*, doi: 10.1016/j.sse.2021.108010, Apr 2021.

80. M.-Y. Kao, Y.-H. Liao, G. Pahwa, A. Dasgupta, S. Salahuddin, and C. Hu, "Energy Storage and Reuse in Negative Capacitance," *IEEE Transactions on Electron Devices*, vol. 68, pp. 1861-1865, Apr 2021.

81. A. Toor, A. Wen, F. Maksimovic, A. M. Gaikwad, K. S. J. Pister, and A. C. Arias, "Stencil-printed Lithium-ion micro batteries for IoT applications," Nano Energy, vol. 82, p. 105666, Apr 2021.

82. X. Wu, J. Zhu, J. W. Evans, C. Lu, and A. C. Arias, "A Potentiometric Electronic Skin for Thermosensation and Mechanosensation," *Advanced Functional Materials*, vol. 31, p. 2010824, Apr 2021.

83. L. P. Tatum, U. Sikder, and T.-J. K. Liu, "Design Technology Co-Optimization for Back-End-of-Line Nonvolatile NEM Switch Arrays," *IEEE Transactions on Electron Devices*, vol. 68, pp. 1471-1477, Apr 2021.

84. Z. Hong, S. Das, C. Nelson, A. Yadav, Y. Wu, J. Junquera, L.-Q. Chen, L. W. Martin, and R. Ramesh, "Vortex Domain Walls in Ferroelectrics," *Nano Letters*, vol. 21, pp. 3533-3539, Apr 2021.

85. J. Xu, S. Kim, B. Nikolic, and Y. S. Shao, "Memory-Efficient Hardware Performance Counters with Approximate-Counting Algorithms," *2021 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp. 226-228, Apr 2021.

86. S. Sayed, S. Hong, X. Huang, L. Caretta, A. S. Everhardt, R. Ramesh, S. Salahuddin, and S. Datta, "Unified Framework for Charge-Spin Interconversion in Spin-Orbit Materials," *Physical Review Applied*, vol. 15, p. 054004, May 2021.

3.5 Technology Transfer

3.5.1 Patents and Patent Applications

June 2020 – May 2021

US Patent 10,690,628
Pens for biological micro-objects
K. T. Chapman, I. Y. Khandros, G. L. Mathieu, J. T. Nevill, M. C. Wu
Patent Granted Date: June 23, 2020

US Patent 10,715,887
Silicon-photonics-based optical switch with low polarization sensitivity
T. J. Seok, H. A. N. Sangyoon, M. C. A. Wu
Patent Granted Date: July 14, 2020

US Patent 10,935,776
Three-dimensional scanless holographic optogenetics with temporal focusing
L. Waller, H. Adesnik, N. C. Pégard
Patent Granted Date: March 2, 2021

US Patent App. 16/958,676
Inversion layer gas sensors using bulk silicon chemical sensitive transistors
A. Javey, H. M. Fahad, N. Gupta
Application Publ. Date: March 4, 2021

US Patent 10,964,468
Magnetic memory structures using electric-field controlled interlayer exchange coupling (IEC) for magnetization switching
S. Salahuddin, S. Sayed
Patent Granted Date: March 30, 2021

US Patent App. 17/252,671
Beam-steering System Based on a MEMS-Actuated Vertical-Coupler Array
X. Zhang, M. C. A. Wu, A. S. Michaels, J. Henriksson
Application Publ. Date: April 22, 2021

3.5.2 Available Technologies

Tech ID: 29091
Printed All-Organic Reflectance Oximeter Array
BETR Faculty: Ana Claudia Arias

Tech ID: 27270
Simultaneous Doctor Blading of Different Colored Organic Light Emitting Diodes
BETR Faculty: Ana Claudia Arias

Tech ID: 25799
Optical Phase Retrieval Systems Using Color-Multiplexed Illumination
BETR Faculty: Laura Waller

Tech ID: 25573
Enhancing Photoluminescence Quantum Yield for High Performance Optoelectrics
BETR Faculty: Ali Javey

Tech ID: 25105
Compressive Plenoptic Imaging
BETR Faculty: Laura Waller

Tech ID: 24720
System for Patterned Illumination Microscopy
BETR Faculty: Laura Waller

Tech ID: 24717
Enhanced Patterning of Integrated Circuits
BETR Faculty: Tsu-Jae King Liu

Tech ID: 24507
Solution Processed Flexible Near-Infrared Organic Light Emitting Diodes and Organic Photodetectors for Wearable Sensors
BETR Faculty: Ana Claudia Arias

Tech ID: 24184
Chemical-Sensitive Field-Effect Transistor
BETR Faculty: Ali Javey

Tech ID: 24171
LED array Microscopy Using Multiplexed Illumination Methods and Software
BETR Faculty: Laura Waller

Tech ID: 23976
Partially Coherent Phase Recovery by Kalman Filtering
BETR Faculty: Laura Waller

Tech ID: 23955
A Thin Film VLS Semiconductor Growth Process
BETR Faculty: Ali Javey

Tech ID: 23488
Printed Organic LEDs And Photodetector for A Flexible Reflectance Measurement-Based Blood Oximeter
BETR Faculty: Ana Claudia Arias

Tech ID: 23092
Micro Electromechanical Switch Design with Self Aligning and Sub-Lithographic Properties
BETR Faculty: Tsu-Jae King Liu

Tech ID: 22395
Concave Nanomagnets With Widely Tunable Anisotropy Properties
BETR Faculty: Jeffrey Bokor

Tech ID: 18962
Improved Mechanical Contact Reliability and Energy Efficiency for CMOS Applications
BETR Faculty: Tsu-Jae King Liu

Tech ID: 18103
Nanowire-based Chemical Connector for Miniature-Scale Applications
BETR Faculty: Ali Javey

Tech ID: 17830
Low Cost, Low-Temperature Polycrystalline Semiconductor Films for Solar Cells and Large Scale Integrated Circuits
BETR Faculty: Tsu-Jae King Liu

Tech ID: 17658
Ultra-low-power And Robust Integrated Circuits for Logic And Memory
BETR Faculty: Tsu-Jae King Liu

Tech ID: 17609
Nano-electro-mechanical Non-volatile Memory (nemory)
BETR Faculty: Tsu-Jae King Liu

Tech ID: 17370
Low Voltage Mems Flash Memory
BETR Faculty: Tsu-Jae King Liu

Tech ID: 17319
Platform for Batch Integration Of Dissociated Or Incompatible Technologies
BETR Faculty: Tsu-Jae King Liu

Tech ID: 17172
Improved DRAM With Capacitorless Double-gate
BETR Faculty: Tsu-Jae King Liu

Tech ID: 16952
A Method for Forming Double-gate Metal Oxide Semiconductor Field Effect Transistors
BETR Faculty: Tsu-Jae King Liu, Jeffrey Bokor

4 Appendices

Appendix A: Abstracts of Research Seminars/Webinars ……..…… 63

Appendix B: Agenda of 2020 Spring BETR Center Workshop ……..… 84

Appendix C: Agenda of 2020 Fall BETR Center Workshop …….. 85

A Survey of Emerging Beyond CMOS Devices and Architectures

Sapan Agarwal
Senior Member of Technical Staff
Sandia National Laboratories

July 23, 2020

Abstract: As the fundamental limits of conventional digital transistors are reached, new devices, architectures and computing paradigms are needed to enable orders of magnitude improvements in energy efficiency and latency. The International Roadmap for Devices and Systems (IRDS) is a set of predictions for emerging electronics and serves as the successor to the ITRS. This talk will give an overview of the Beyond CMOS chapter of IRDS. First, emerging non-volatile memories and transistors that are intended to be drop-in replacements for existing CMOS based technologies will be briefly reviewed. Next, emerging architectures and computing paradigms will be reviewed. This includes analog crossbar-based computing architectures, neuro-inspired computing, computing with dynamical systems, probabilistic computing, and reversible computing. These architectures will require co-design between devices, circuits, architectures and algorithms.

Bio: Dr. Sapan Agarwal is a Senior Member of Technical Staff at Sandia National Laboratories. He is leading projects to develop analog in-memory computing accelerators for high performance computing, database accelerators, and neural network training and inference. He is also leading the development of simulation tools to model the impact of device level radiation events on a running algorithm. He created CrossSim, a crossbar simulator for analog neural network accelerators that allows for the co-design of novel devices and algorithms by modeling the impact of device properties on neural algorithms. He also created AWE-ML (averaged weights for explainable machine learning), a new classifier that allows for machine learning predictions to be interpreted. He has invented several new semiconductor device concepts including new low power transistors, artificial analog synapses, and wide band gap LEDs. He works with the IEEE International Roadmap for Devices and Systems to map out future computing architectures and devices.

BETR Solid State Technology and Devices Seminar

Sensing Quantum Materials with New Electromagnetic Probes

Dr. Eric Yue Ma
Department of Applied Physics
Stanford University

September 18, 2020

Abstract: The interaction between electromagnetic fields and condensed matter not only underpins much of modern technology, but also provides one of the most fundamental ways to study quantum materials. To this end, the ever expanding family of emerging phenomena in these materials calls for new electromagnetic probes working in unexplored parameter spaces. In this talk I will present two of such cases where deeply sub-wavelength probes allowed us to study interesting physics at length scales millions of time smaller than the corresponding free-space wavelength: Metallic magnetic domain walls in a magnetic insulator as a new class of interface states established by microwave impedance microscopy, and ultrafast charge transfer across a sub-nm van der Waals interface probed by time-domain THz emission spectroscopy. I will also discuss the exciting opportunities provided by advancing and combining several of these techniques to create an integrated extreme-broadband imaging and sensing system.

Bio: Dr. Eric Y. Ma received his B.S. in Physics from Peking University, and his Ph.D. in Applied Physics from Stanford University. He stayed at Stanford as a joint post-doctoral researcher in Applied Physics and Electrical Engineering. He has also held positions at Apple. Dr. Ma will join Berkeley Physics full time as an Assistant Professor in July 2021.

BETR Solid State Technology and Devices Seminar

Stackable Electronics Enabled by Freestanding 2D/3D Materials

Prof. Jeehwan Kim
Department of Mechanical Engineering
Department of Materials Science and Engineering
Massachusetts Institute of Technology

Friday, September 25, 2020

Abstract: 2D material-based devices have received great deal of attention as they can be easily stacked to obtain multifunctionality. With their ultrathin thicknesses, such multifunctioning devices become so flexible and conformal that they can be placed onto any 3D featured surfaces. However, 2D heterostructures are typically demonstrated as stacked flakes where single or few devices can be fabricated due to lack of strategies for layer-by-layer stacking of 2D materials at the wafer scale. In this talk, I will discuss our unique strategy to isolate wafer-scale 2D materials into monolayers and stack them into a heterostructure by using a layer-resolved splitting (LRS) technique [1]. This technique enables my group at MIT to explore unprecedented wafer-scale 2D heterodevices including integrated photonics, 3D neuromorphic computing, and microLEDs, which will be introduced in my talk. While 2D heterostructures promise interesting futuristic devices, the performance of 2D material-based devices is substantially inferior to that of conventional 3D semiconductor materials. However, 3D materials exist as their bulk form, thus it is challenging to stack them together for heterostructures. Obviously, conformal coating of such single-crystalline bulks on 3D features is impossible. My group at MIT has recently invented a 2D materials-based layer transfer (2DLT) technique that can produce single-crystalline freestanding membranes from any compound materials with their excellent semiconducting performance [2-4]. This technique is based on remote epitaxy of single-crystalline films on graphene followed by peeling from graphene. Stacking of freestanding 3D material membranes will enable unprecedented 3D heterostructures whose performance is expected to be superior to that of 2D heterostructures. I will talk about our group's effort to apply single-crystalline freestanding membranes for flexible, conformal electronics as well as for 3D heterostructures. Finally, I will conclude my talk by discussing perspectives of coupling 2D-3D freestanding membranes for 2D-3D mixed heterostructured devices that can be enabled by our LRS and 2DLT techniques [5,6].

References

[1] J. Shim, S. Bae, et al, and J. Kim, "Controlled crack propagation for atomic precision handling of wafer-scale two-dimensional materials" Science, 362, 665 (2018). [2] Y. Kim, et al, and J. Kim, "Remote epitaxy through graphene enables two-dimensional material based layer transfer" Nature, Vol. 544, 340 (2017). [3] W. Kong, et al, and J. Kim, "Polarity governs atomic interaction through two-dimensional materials", Nature Materials, Vol. 17, 999 (2018). [4] S. Bae et al, and J. Kim, "Graphene-assisted spontaneous relaxation towards dislocation-free heteroepitaxy", Nature Nanotechnology, published online (2020). [5] S. Bae, et al, and J. Kim, "Integration of bulk materials with two-dimensional materials for physical coupling and applications", Nature Materials (2019). [6] H. Kum, et al., J. Kim, "Heterogeneous integration of single-crystalline complex-oxide membranes, Nature, Vol 578, 75-81 (2020).

Bio: Dr. Jeehwan Kim is an Associate Professor of Massachusetts Institute of Technology in the Mechanical engineering and Materials Science and Engineering. He is a Principal Investigator in Research Laboratory of Electronics at MIT. Prof. Kim's group focuses on innovation in nanotechnology for next generation computing and electronics. Before joining MIT in 2015, he was a Research Staff Member at IBM T.J. Watson Research Center in Yorktown Heights, NY since 2008. Many of his patents have been licensed for commercialization. Prof. Kim is a recipient of 20 IBM high value invention achievement awards. In 2012, he was appointed a "Master Inventor" of IBM in recognition of his active intellectual property generation and commercialization of his research. He is a recipient of DARPA Young Faculty Award. He is an inventor of 200 issued/pending US patents and an author of 50 articles in peer-reviewed journals. He received his B.S. from Hongik University, his M.S. from Seoul National University, and his Ph.D. from UCLA in 2008, all of them in Materials Science.

Use of the Roadmap (IRDS) Method to Overcome Industry Inflection Points

Dr. Paolo A. Gargini
IEEE-Life Fellow, JSAP Fellow
Chairman IRDS
Former Director of Technology Strategy (Intel 1978-2012)

Friday, October 9, 2020

Abstract: In 1965 Gordon Moore, co-founder of Fairchild Semiconductors and also Intel Corporation, predicted that the number of transistors per die would double every year until 1975 if specific actions were taken to eliminate any inflection points. By 1975 data showed his predictions to be correct. He then predicted that the number of transistors would double every two years for the foreseeable future if appropriate actions were taken. Following Gordon Moore's demonstrated success of the roadmap methodology, the National Technology Roadmap for Semiconductors was formed in 1991; the roadmap became international (ITRS) in 1998. Following the ITRS recommendations the semiconductor industry introduced in a timely fashion High-K/Metal-Gate and FinFET into manufacturing. Beginning with 2016 the scope of the roadmap was extended to also include systems trends. New recommendations for actions to be taken in the next 15 years have been formulated.

Bio: Dr. Paolo Gargini was born in Florence, Italy and received a doctorate in Electrical Engineering in 1970 and a doctorate in Physics in 1975. He was a researcher at Stanford University and at Fairchild Camera and Instrument in Palo Alto in the early 70s. He joined Intel in 1978, responsible for MPU technology (e.g., 80286 and the 80386). In 1985, he headed the first submicron team. In 1996, he became Director of Technology Strategy, Intel Fellow; responsible for worldwide consortia research from 1993 to 2012; member of Sematech, SRC and SIA Boards, Chairman of the NRI. Dr. Gargini led the industry-wide conversion to 300mm wafers as Chairman of the I300I initiative. From 1998 to 2015, Dr. Gargini was Chairman of the ITRS sponsored by the WSC. Since 2016 he is the Chairman of the IRDS sponsored by IEEE. He is co-chairman of the EUVL Symposium. Dr. Gargini was inducted in the VLSI Research Hall of Fame in 2009, IEEE Fellow in 2009, IEEE Life-Fellow in 2020 and JSAP Fellow in 2014. He is a member of the Leadership Team of the International Network Generations Roadmap (INGR), an IEEE initiative.

BETR Solid State Technology and Devices Seminar

Electric Field Control of Magnetism

Prof. Ramamoorthy Ramesh
Department of Physics & Department of Materials Science and Engineering
Lawrence Berkeley National Laboratory
University of California, Berkeley

Friday, October 16, 2020

Abstract: Complex perovskite oxides exhibit a rich spectrum of functional responses, including magnetism, ferroelectricity, highly correlated electron behavior, superconductivity, etc. The basic materials physics of such materials provide the ideal playground for interdisciplinary scientific exploration with an eye towards real applications. Over the past decade the oxide community has been exploring the science of such materials as crystals and in thin film form by creating epitaxial heterostructures and nanostructures. Among the large number of materials systems, there exists a small set of materials which exhibit multiple order parameters; these are known as multiferroics, particularly, the coexistence of ferroelectricity and some form of ordered magnetism (typically antiferromagnetism). The scientific community has been able to demonstrate electric field control of both antiferromagnetism and ferromagnetism at room temperature. Current work under the SRC-JUMP program is focused on ultralow energy (1 attoJoule/operation) electric field manipulation of magnetism as the backbone for the next generation of ultralow power electronics. We are exploring many pathways to get to this goal. In this talk, I will describe our progress to date on this exciting possibility. The talk will conclude with a summary of where the future research is going.

Bio: Dr. Ramamoorthy Ramesh is the Purnendu Chatterjee Chair Professor in the Departments of Physics & Materials Science and Engineering at the University of California, Berkeley. He pursues key materials physics and technological problems in complex multifunctional oxides. Using conducting oxides, he solved the 30-year enigma of polarization fatigue in ferroelectrics. He pioneered research into manganites coining the term, Colossal Magnetoresistive (CMR) Oxides. His work on multiferroics demonstrated electric field control of ferromagnetism, a critical step towards ultralow power memory and logic elements. His extensive publications on the synthesis and materials physics of complex oxides are highly cited (over 65,000 citations, H-factor =110). He is a fellow of APS, AAAS & MRS and an elected member of the U.S. National Academy of Engineering and a Foreign member of the Royal Society of London. His awards include the Humboldt Senior Scientist Prize, the APS Adler Lectureship and McGroddy New Materials Prize, the TMS Bardeen Prize and the IUPAP Magnetism Prize and Neel Medal. He was recognized as a Thomson-Reuters Citation Laureate in Physics for his work on multiferroics. He served as the Founding Director of the successful Department of Energy SunShot Initiative in the Obama administration, envisioning and coordinating the R&D funding of the U.S. Solar Program, spearheading the reduction in the cost of Solar Energy. He also served as the Deputy Director of Oak Ridge National Laboratory and the Associate Lab Director at LBNL.

Low Thermal Budget Trends for Interconnect RDL Polyimides For 3D Advanced IC Backend Applications

Dr. Zia Karim
Sr. Vice President and Chief Marketing Officer (CMO)
Yield Engineering Systems (YES)

Friday, October 23, 2020

Abstract: In the ongoing effort to extend and move beyond Moore's Law, advances in backend IC processing are extending the capabilities of heterogeneous and 3D integration. 3D stack memory has already fueled considerable progress in 3D integration, enabling high-bandwidth memory (HBM) and dynamic random-access memory (DRAM). In addition to the 3D stacking ofmemory, 3D system integration allows a variety of chiplets and other components to bestacked, delivering high compute density and high performance at low cost. Multi-layer RDLs(Redistribution layers) are used to connect these dissimilar chips on organic, glass, silicon or fan-out substrates. The need to transition to all-Cu interconnect as well as to manage fan-out stress has resulted in a temperature limit of 250°C for large numbers of these products. Consequently, process technology for Polyimide, Photo Imageable Dielectric (PID) and Photo Sensitive Polyimide (PSPI) must now enable a faster cure at lower temperatures resulting in lower thermal budget, while also delivering better film properties. In this seminar, the physical, mechanical, thermal, and electrical properties of different types of Polyimide and Poly-Benz-Oxazole (PBO) materials, were studied as a function of different process parameters, under atmospheric and vacuum process conditions. Vacuum cure even in lower temperatures resulted in higher thermal stability, lower outgassing, and better thermal properties. In electrical characterization, vacuum cure showed better dielectric strength as well as lower dissipation factor. These results are consistent with the assumption that cure under vacuum reduces the amount of volatile and volatilizable material remaining in the film after the cure process. The use of sub-atmospheric curing or annealing technology at low temperature improved both the quality and the performance of the cured polyimide films for RDL applications that are relevant to the multi-level metallization process of Fan Out Wafer Level Packaging (FOWLP) and Fan Out Panel Level Packaging (FOPLP), and therefore to 3D stack integration.

Bio: Dr. Zia Karim is currently Sr. Vice President and Chief Marketing Officer (CMO) at Yield Engineering Systems, a leading Semiconductor Equipment Company for Backend Advanced IC Packaging Processes. Dr. Karim most recently was Vice President of Business Development and Technology at AIXTRON/Genus (acquisitions) where he worked for over 15 years. Dr. Karim has held senior management positions in Applied Materials, and Novellus (acquired by LAM Research) after he started his career in Sharp Microelectronics in 1994. Dr. Karim recently completed Certificate of Business Excellence in Executive Education from UC Berkeley Hass School of Business. Dr. Karim received Ph.D, in Electronic Engineering from Dublin City University in Ireland, and B.Sc and M.Sc degree from Bangladesh University of Engineering and Technology in Electrical and Electronic Engineering. Dr. Karim took a pioneering role in positioning W/WSi CVD, Low k PECVD, High K ALD, and III-V MOCVD process in Semiconductor Logic and Memory Devices. Dr. Karim owns sixteen (16) patents. Other than organizing or co-organizing several Conferences, Symposiums and related Transactions, Dr. Karim also authored more than forty (40) published papers.

BETR Solid State Technology and Devices Seminar

Emerging Materials and Devices for Energy Harvesting Applications

Prof. Derya Baran
Materials Science and Engineering
KAUST Solar Center
King Abdullah University of Science and Technology (KAUST)

Friday, November 6, 2020

Abstract: Energy harvesting as well as storage is emerging as a viable method for electronic devices to utilize ambient energy from the surrounding environment and convert it into electrical energy for storage. This technology offers devices that has the potential to serve as an alternative power supply instead of batteries that are ubiquitous in IoT devices, autonomous wireless devices such as in wearables and sensors. Conventional devices require vacuum based technologies to be produced which brings energy intense production and tedious processing methods. Solution- processed semiconductors including organic materials, metal-halide perovskites and quantum dots — have recently emerged as candidates for next-generation energy harvesting devices. They combine ease of processing, controllable optoelectronic properties, facile integration with complementary metal–oxide–semiconductors, compatibility with flexible substrates and good performance. They offer flexibility, stretchability and even healability are promising for such future devices used for sensors, printed circuits, printed diagnostics etc. This talk will focus on the state of the art of solution processed emerging materials and enabled devices for energy conversion and harvesting. In particular, solar cells and thermoelectric materials and devices will be elaborated and their suitability for printed electronics will be discussed.

Bio: Dr. Derya Baran, originally from Turkey, is a passionate scientist who received her doctorate degree from Friedrich-Alexander Erlangen-Nürnberg University in Materials Science and Engineering in 2014. Since 2017, she is an assistant professor at King Abdullah University of Science and Technology (KAUST), Saudi Arabia. Her research group (OMEGALAB) focus on engineering organic and hybrid materials for energy harvesting devices. Derya co-authored more than 100 publications including Nature Materials, Nature Materials Reviews, Science etc. and is a recipient of Helmholtz Association postdoc grant in 2015 (joint with Imperial College London). She was selected for MIT Technology Review's 2018 list of '35 Innovators under 35' for her development of transparent power glass that can generate electricity and block the heat for greenhouses and future buildings. As a scientist and entrepreneur, she strives to be a role model to younger generations.

Robust and Energy-Efficient VLSI Silicon Photonics for Communications and Computing

Dr. Di Liang
Large-Scale Integrated Photonics Lab
Hewlett Packard Enterprise

Friday, February 12, 2021

Abstract: The ending decade of 2010s is an era when cloud-driven data centers and photonic interconnects, particularly silicon photonics, enable each other to scale. Same promise is held to develop interconnect solutions with energy efficiency, large bandwidth, low latency, and affordable cost for next-generation high-performance computing. To fulfil this mission, innovative materials, device structures, integration platform, and link architecture were extensively studied in Hewlett Packard Labs. I will review our recent progress in developing robust WDM transceivers on silicon and potential to extend integrated silicon photonics into the optical computing domain.

Bio: Dr. Di Liang is a Distinguished Technologist and Research Manager at Hewlett Packard Labs in Hewlett Packard Enterprise (HPE). He leads the advanced R&D in silicon and III-V integrated photonics for HPE's server and high-performance computing business. He is currently a principal investigator for several federally funded R&D programs. Prior to joining HP Labs, he was a research specialist at UCSB and was a core member in early-stage development of the hybrid III/V-on-silicon platform which has been commercialized successfully. He has authored and co-authored over 220 journal and conference papers with over 5200 citations, 6 book chapters, and was granted by 45 patents with another 50+ pending. He is an associated editor for IEEE Journal of Quantum Electronics and OSA Photonics Research Journals. He is a Fellow of OSA, a senior member of IEEE and a member of SPIE.

BETR Solid State Technology and Devices Seminar

News and Future of Semiconductors

Prof. Chenming Hu
TSMC Chair Professor Emeritus
Electrical Engineering and Computer Science
UC Berkeley

Friday, February 19, 2021

Abstract: Semiconductors are in the news--technology, financial and political news. It is recognized as a force that changed and continues to change the world. At the same time, its own future and what to do about its future are being questioned by the public, students, researchers and governments. This talk will look at some of the questions and will leave time for audience questions.

Bio: Dr. Chenming Hu is called the Father of 3D Transistor for developing the FinFET in 1999. Intel is the first company to use FinFET in 2011 calling it the most radical shift in semiconductor technology in over 50 years. Soon, all computers, smart phones, and the internet ran on FinFET processors. He received the US National Technology and Innovation Medal from President Obama in 2016. He leads the ongoing development of BSIM, a suite of industry standard transistor models. University of California provides it loyalty free for industry to design integrated circuits worth well over a trillion US dollars since 1995. IEEE, the world's largest technology association, gave him its highest award, Medal of Honor, in 2020 for helping to "keep Moore's Law going over many decades" after calling him "Microelectronics Visionary" for "achievements critical to producing smaller yet more reliable and higher-performance integrated circuits" in 2009. Electronic Design Automation industry's 2013 Kaufman Award noted his "tremendous career of creativity and innovation that fueled the past four decades of the semiconductor industry". Dr. Hu is TSMC Distinguished Chair Professor Emeritus of University of California, Berkeley. From 2001 to 2004 he was the Chief Technology Officer of TSMC, world's largest dedicated integrated circuits manufacturing company. He was the board chairman of the nonprofit Friends of Children with Special Needs and the East Bay Chinese School. He has authored six books including a semiconductor device textbook and 1000 research papers, and has been granted over 100 US patents. He is honored with memberships in the US National Academy of Engineering, Chinese Academy of Sciences, US Academy of Inventors and Academia Sinica. His other professional honors include the IEEE Jack Morton Award, Solid State Circuits Award, and Nichizawa Medal; Asian American Engineer of the Year Award, Silicon Valley Engineering Hall of Fame, Honorary Doctoral Degree of National Chiao Tung University and the IEEE EDS Education Award for "distinguished contributions to education and inspiration of students, practicing engineers and future educators". He also received UC Berkeley's highest honor for teaching — the Berkeley Distinguished Teaching Award. Dr. Hu received his B.S. degree from National Taiwan University, which honored him with its Distinguished Alumni Award, and M.S. and Ph.D. degrees from UC Berkeley. He shares an interest in painting with his sons Raymond and Jason.

BETR Solid State Technology and Devices Seminar

Ubiquitous Active Surfaces

Vladimir Bulović
Professor and Fariborz Maseeh Chair in Emerging Technology
Electrical Engineering and Computer Science
MIT

Friday, February 26, 2021

Abstract: Paper-thin devices can turn everyday surfaces into light emitters, solar collectors, mechanical sensors, audio and ultra-sound speakers, augmenting the utility of present environments and opening pathways for new portable and large-scale technologies. Proliferation of such active surfaces necessitates a paradigm shift in device design and an introduction of new fabrication processes. Through examples, the talk will show that with recent advancements in the use of molecular, polymeric and quantum dot thin films, both the paper-thin device technology and the scalable fabrication processes are on the horizon, ushering scalable proliferation of ubiquitous active surfaces.

Bio: Dr. Vladimir Bulović is a Professor of Electrical Engineering at the Massachusetts Institute of Technology, holding the Fariborz Maseeh Chair in Emerging Technology. He directs the Organic and Nanostructured Electronics Laboratory, co-leads the MIT-Eni Solar Frontiers Center, leads the Tata GridEdge program, and is the Founding Director of MIT.nano, MIT's new nano-fabrication, nano-characterization, and prototyping facility. He is an author of over 250 research articles (cited over 50,000 times and recognized as the top 1% of the most highly cited in the Web of Science). He is an inventor of over 120 U.S. patents in areas of light emitting diodes, lasers, photovoltaics, photodetectors, chemical sensors, programmable memories, and micro-electro machines, majority of which have been licensed and utilized by both start-up and multinational companies. The three start-up companies Bulović co-founded jointly employ over 350 people, and include Ubiquitous Energy, Inc., developing nanostructured solar technologies, Kateeva, Inc., focused on development of printed electronics, and QD Vision, Inc. (acquired in 2016) that produced quantum dot optoelectronic components. Products of these companies have been used by millions. Bulović was the first Associate Dean for Innovation of the School of Engineering and the Inaugural co-Director of MIT's Innovation Initiative, which he co-led from 2013 to 2018. For his passion for teaching Bulović has been recognized with the MacVicar Fellowship, MIT's highest teaching honor. He completed his Electrical Engineering B.S.E. and Ph.D. degrees at Princeton University.

BETR Solid State Technology and Devices Seminar

Silicon Photonics: The Bumpy Road Toward Industrial Success

Gianlorenzo Masini
Luxtera/Cisco

Friday, March 5, 2021

Abstract: In the sizzling Roman summer of 1997, Giovanni, Lorenzo, and I hijacked the home-brewed CVD chamber in the Physics Department of University Roma Tre to deposit our first relaxed Ge on Si sample. The lab Director was on vacation (as every Italian holding a permanent job position in the month of August would be), so he could not stop us from fully draining a (very) expensive GeH4 cylinder for our crazy experiment: building an NIR photodetector right on top of a silicon chip. Surprisingly, the device worked right away: certainly leaky but fast and responsive - almost good enough for making transceivers. This is just one of the stories, accumulated over the many years, that has grafted a new and unique 'species' into the silicon mainstream industry tree: a branch that is finally bearing fruits in the form of state-of-the-art high-speed transceivers, and will likely soon diversify into other areas (AI, Automotive to mention a couple). Growing has not been easy: the only remarkable quality of Si, from an integrated optics standpoint, is its high index. Everything else is dismal: indirect bandgap, no linear absorption in the telecom bands (but strong two-photon absorption), small, or non-existing electro-optic coefficients, and the list goes on and on. But then there is the silicon manufacturing knowledge and infrastructure: decades and hundreds of billions invested in the development of an industry that is capable today of delivering devices with features just a little larger than a few atomic radiuses to billions of customers. That was the bet: directing the CMOS beast to tame silicon into riding with optics. Today, we can say with some certainty that it was a good bet. This seminar will elucidate a few of the key milestones, mistakes, and achievements along the road, as seen by someone that was lucky enough to ride on it for the last couple of decades.

Bio: Dr. Gianlorenzo Masini earned his Laurea and Ph.D. degrees from the University “La Sapienza” of Roma, Italy in 1991 and 1993, respectively. From 1994 to 2004 he taught and performed research at the University “Roma Tre”. While there, he pioneered the use of relaxed Ge on Si in high-performance photodetectors for the near infrared. In 2004 he joined Luxtera, a California startup dedicated to the development of Silicon Photonics optical transceivers. At Luxtera, eventually acquired by Cisco in 2019, he contributed to the development of several aspects of the technology and of the devices used in its best-selling transceivers. Dr. Masini co-authored more than 150 papers, 25 granted patents, and 3 book chapters.

BETR Solid State Technology and Devices Seminar

Organic Mixed Ionic/Electronic Conductors for Applications in Bioelectronics

Jonathan Rivnay
Assistant Professor
Department of Biomedical Engineering
Northwestern University

Friday, March 12, 2021

Abstract: Direct measurement and stimulation of ionic, biomolecular, cellular, and tissue-scale activity is a staple of bioelectronic diagnosis and/or therapy. Bi-directional interfacing can be enhanced by a unique set of properties imparted by organic electronic materials. These materials, based on conjugated polymers, can be adapted for use in biological settings and show significant molecular-level interaction with their local environment, readily swell, and provide soft, seamless mechanical matching with tissue. At the same time, their swelling and mixed ionic/electronic conduction allows for enhanced ionic-electronic coupling for transduction of biosignals. These properties serve to enable new capabilities in bioelectronics. In the first part of my talk, I will focus on the design of polymer bioelectronic materials for enhanced electrophysiological sensors based on electrochemical transistors. Synthetic design and processing can yield high performance mixed conductors with large volumetric capacitance, high transconductance, and steep subthreshold switching characteristics for low power sensing. I will then discuss recent interest in developing devices and simple circuits based on electrochemical transistors that would impart added functionality to sensing sites and ease the burden on back-end electronics for signal processing and analysis. These developments highlight the role of materials design for addressing critical needs in bio-electronic interfacing.

Bio: Dr. Jonathan Rivnay earned his B.Sc. in 2006 from Cornell University (Ithaca, NY). He then moved to Stanford University (Stanford, CA) where he earned a M.Sc. and Ph.D. in Materials Science and Engineering studying the structure and electronic transport properties of organic electronic materials. In 2012, he joined the Department of Bioelectronics at the Ecole des Mines de Saint-Etienne in France as a Marie Curie post-doctoral fellow, working on conducting polymer-based devices for bioelectronics. Jonathan spent 2015-2016 as a member of the research staff in the Printed Electronics group at the Palo Alto Research Center (Palo Alto, CA) before joining the Department of Biomedical Engineering at Northwestern University in 2017. He is a recipient of an NSF CAREER award, ONR Young Investigator award, and has been named an Alfred P. Sloan Research Fellow, and MRS Outstanding Early Career Investigator.

BETR Solid State Technology and Devices Seminar

Engineering (Useful) Quantum Systems

Sara Mouradian
Intelligence Community Postdoctoral Fellow
Department of Physics
UC Berkeley

Friday, March 19, 2021

Abstract: Quantum technologies have the potential to revolutionize sensing, communication, and computation. To realize this potential, it will be necessary to scale the size and complexity of engineered quantum systems by several orders of magnitude without sacrificing coherence or fidelity. Trapped ion qubits provide unparalleled coherence and are a leading platform for current small-scale quantum technology demonstrations. Optical addressing of individual ions with low crosstalk enables high-fidelity single and multi-qubit gates, and ions trapped in the same potential naturally allow for all-to-all connectivity. However, free-space control and routing of these optical control fields presents a scaling challenge. I will focus on requirements for a deployable trapped-ion quantum sensor and introduce an integrated photonics control platform for parallel laser delivery which will increase stability, reduce size, and allow us to increase the number of sensors measured in parallel without sacrificing fidelity. Finally, I will present a path towards a modular trapped-ion quantum processor with active integrated photonics for control within each module, and high fidelity physical and optical links between modules.

Bio: Dr. Sara Mouradian is an Intelligence Community Postdoctoral Fellow at the University of California, Berkeley in the Ion Trap Group working to build useful quantum technologies based on trapped ions. She is interested in building robust and scalable infrastructure for the large-scale quantum technologies that are necessary for the next generation of computing, communication, and sensing. She received her PhD in Electrical Engineering and Computer Science in the Quantum Photonics Laboratory at MIT working on scalable integrated architectures and diamond nanophotonics for quantum information processing with nitrogen vacancy centers in diamond. Her thesis won both the Dmitris N. Chorafas and the MIT Microsystems Technology Laboratory Dissertation Awards. Her master's work was done in the Optical and Quantum Communications Group at MIT where she built the first demonstration of quantum illumination in the optical domain.

BETR Solid State Technology and Devices Seminar

Quantum Interconnects for Superconducting Quantum Processors

Alp Sipahigil
Assistant Professor
Electrical Engineering and Computer Sciences
UC Berkeley

Friday, April 2, 2021

Abstract: The ability to store, transfer, and process quantum information promises to transform how we calculate, communicate, and measure. In the past two decades, superconducting microwave circuits based on Josephson junctions emerged as a powerful platform for quantum computation. However, these systems operate at low temperatures and microwave frequencies, and require coherent optical interconnects to transfer quantum information across long distances. In this talk, I will present our recent experiments demonstrating the transduction of a superconducting qubit excitation to an optical photon. I will present an integrated device platform combining superconducting qubits, piezoelectric transducers, and optomechanical transducers for converting quantum states between superconducting circuits, single phonons, and single optical photons. I will discuss how we use nanomechanical oscillators in their quantum ground states to convert single photons from microwave frequencies to the optical domain. I will conclude by discussing the prospects of this approach for realizing future quantum communication networks based on superconducting quantum processors, and discuss our plans on acoustic engineering of superconducting quantum processors for improved quantum coherence and protection from cosmic ray events.

Bio: Dr. Alp Sipahigil is the Chang Hui Faculty Fellow and an Assistant Professor of Electrical Engineering and Computer Sciences at the University of California, Berkeley. He has joint appointments as a Faculty Scientist at the Materials Sciences Division at Lawrence Berkeley National Laboratory and a supporting appointment at UC Berkeley Physics. His research is in solid-state quantum technologies, with a focus on hybrid quantum devices based on superconducting qubits, nanomechanics, nanophotonics, and atom-like defects in solids. Prior to joining Berkeley in 2021, he was an Institute for Quantum Information and Matter postdoctoral scholar at Caltech. He received his Ph.D. in Physics from Harvard University in 2017 and his B.S. degrees in Physics and Electrical Engineering from Bogazici University in 2010.

BETR Solid State Technology and Devices Seminar

The Hunt for Mobile Holes Induced by Polarization in GaN

Huili Grace Xing
William L. Quackenbush Professor
Electrical and Computer Engineering
Materials Science and Engineering
Cornell University

Friday, April 9, 2021

Abstract: Two-dimensional electron gas (2DEG) in the GaN semiconductor family can be readily induced by polarization discontinuity without impurity dopants at a heterointerface, which is the heart of a high-electron mobility transistor (HEMT). Over the past decade, GaN HEMTs have been employed in 5G base stations, faster and miniature battery chargers etc. thanks to the high-speed operation and high power density afforded by this semiconductor family. As a fundamental departure from impurity-doping and modulation-doping, the two well-known doping schemes in semiconductors, polarization-induced three-dimensional electron gas in GaN was also postulated and experimentally demonstrated for the first time in 2002 [1]. Thanks to the advent of high-quality bulk GaN substrates, polarization-induced three-dimensional hole gas in GaN was demonstrated in 2010, with assistance of impurity dopants; for the first time, p-type conductivity in GaN was measured down to cryogenic temperatures, 4 Kelvin [2]. This was nearly an impossible feat in impurity-doped p-type GaN due to carrier freeze-out. It has been about 20 years since the existence of mobile holes in GaN heterostructures without impurity dopants, the counterpart of 2DEG, was postulated. Only recently, undisputable experimental observations are achieved in our lab [3]. The long-missing polarization-induced two-dimensional hole gas (2DHG) is finally observed in undoped gallium nitride quantum wells. Experimental results provide unambiguous proof that a 2D hole gas in GaN grown on AlN does not need impurity doping, and can be formed entirely by the difference in the internal polarization fields across the semiconductor heterojunction. The measured 2D hole gas densities, about 4x1013 cm-2, are among the highest among all known semiconductors and remain unchanged down to cryogenic temperatures. Some of the lowest sheet resistances of all wide-bandgap semiconductors are seen. The observed results provide a new probe for studying the valence band structure and transport properties of wide-bandgap nitride interfaces, and simultaneously enable the missing component for gallium nitride-based p-channel transistors for energy-efficient electronics [4].

[1] D. Jena, H. Xing et al., Appl. Phys. Lett. 81(23), 4395-4397 (2002). DOI: 10.1063/1.1526161. [2] J. Simon, H. Xing, D. Jena et al., Science 327, 60 (2010) DOI: 10.1126/science.1183226. [3] R. Chaudhuri, H. Xing, D. Jena et al., Science 365, 1454 (2019) DOI:10.1126/science.aau8623. [4] K. Nomoto et al, IEDM 2020.

Bio: Dr. Huili Grace Xing is currently the William L. Quackenbush Professor of Electrical and Computer Engineering, Materials Science and Engineering at Cornell University. She was with the University of Notre Dame from 2004 to 2014. She received B.S. in physics from Peking University (1996), M.S. in Material Science from Lehigh University (1998) and Ph.D. in Electrical Engineering from University of California, Santa Barbara (2003), respectively. Her research focuses on development of III-V nitrides, 2-D crystals, oxide semiconductors, recently multiferroics & magnetic materials: growth, electronic and optoelectronic devices, especially the interplay between material properties and device development as well as high performance devices, including RF/THz devices, tunnel field effect transistors, power electronics, DUV emitters and memories. She has authored/co-authored 270+ journal papers and 120+ conference proceeding publications including Nature journals, Physical Review Letters, Applied Physics Letters, Electron Device Letters, and IEDM etc. She is a recipient of AFOSR Young Investigator Award, NSF CAREER Award and ISCS Young Scientist Award. She is a fellow of APS.

Integrated Optical Coherence Tomography: continuous physiological monitoring and the era of *Homo augmentus*

Michael S. Eggleston
Data & Devices Group Leader, AI Research Lab
Nokia Bell Labs, Murray Hill

Friday, April 16, 2021

Abstract: The current Internet of Things (IoT) era, bolstered by the rapid expansion of 5G networks, seeks to integrate every place, thing, and person into a connected global network of everything. By the time we reach the 6G era 10 years in the future, the level of hyper-connectivity we're witnessing today will move beyond simply linking "things," extending directly to the human body and mind. This era of *Homo augmentus* will in turn drive unprecedented levels of human and economic productivity. At Nokia Bell Labs, we are developing the devices and artificial intelligence that will seamlessly integrate human physiology into this network to create the future Augmented Human. This involves developing innovative materials, devices, and machine learning techniques that can continuously and non-invasively interface, sense, and actuate the human body. In this talk, I will describe our recent work on integrated Optical Coherence Tomography (OCT), one of the technologies of *Homo augmentus* that we believe will allow for continuous access to our physiological health. Leveraging integrated photonic and MEMs technologies, we have developed the world's first chip-scale swept-source OCT system, achieving 100dB sensitivity at 100kHz A-scan rate and have packaged this into a battery-powered portable device for remote diagnostics. Along with core hardware advances, I will overview the algorithmic and AI techniques we have developed to harness this platform for continuous biophysical monitoring. Finally, I will highlight a novel biochemical sensing technique we have pioneered that leverages OCT and bio-optical transducers to extract chemical information in 3D tissue environments. We believe this platform will form the foundation of future advanced remote health diagnostics such as at-home wound monitoring and infectious disease screening.

Bio: Dr. Michael S. Eggleston received his B.S. degree in Electrical Engineering and Physics from Iowa State University and his Ph.D. in Electrical Engineering from UC Berkeley. In 2015, he joined Nokia Bell Labs in Murray Hill, NJ where he currently leads the Data and Devices Group. An optical device physicist at heart, Michael's research has included investigation into ultra-wideband wireless technologies, solar cells, environmental sensing, optical coherence tomography, low-power optical interconnects and devices, and integrated multi-wavelength lasers. His current research interests are in the creation of technologies that seamlessly integrate human physiology into the digital world. This includes work in battery-less sensing, non-invasive biochemical monitoring, and human-machine interfaces.

BETR Solid State Technology and Devices Seminar

Wearable Platforms for Sweat Sensing at Rest

Mallika Bariya
Javey Research Group
Electrical Engineering and Computer Science
UC Berkeley

Friday, April 23, 2021

Abstract: Sweating is typically associated with exercise, elevated temperatures, or chemical stimulation. However, we also sweat during routine and sedentary activities for thermoregulation, as the body finely controls core temperature. This kind of sweat is secreted at dramatically lower rates and volumes, making it difficult to collect and analyze in wearable platforms. In this talk I'll review our recent efforts to enable sweat analysis at rest, using functionalized glove-based platforms and microfluidic patches. I'll discuss device aspects as well as preliminary subject studies that use these platforms for non-invasive physiological insights.

Bio: Mallika Bariya is a Ph.D. candidate and NSF Graduate Research Fellow in Prof. Ali Javey's group. Her research is focused on electrochemical sensing technologies for healthcare applications, with particular emphasis on developing and using sweat sensors to understand how non-invasive parameters can reflect deeper physiology.

BETR Solid State Technology and Devices Seminar

Electronics 5.0: New Materials and Devices for Edge Intelligence

Tomás Palacios
Department of Electrical Engineering and Computer Science
MIT

Friday, April 30, 2021

NOTE: THIS SEMINAR WILL NOT BE RECORDED.

Abstract: The end of traditional transistor scaling brings unprecedented new opportunities to semiconductor devices and electronics. We are at the onset of a new technology revolution, which will focus on distributed intelligence and will be pushing the limits of edge sensing and computing. This seminar will describe some of our work on new materials and devices to enable this vision, including 1. Gallium Nitride CMOS FinFET amplifiers for much more efficient communications; 2. One-layer-thick molybdenum disulfide wi-fi energy harvesters to enable ubiquitous electronics; and 3. A new generation of cell-sized autonomous electronic microsystems to revolutionize invisible sensing. The seminar will conclude with a reflection on how the democratization of heterogeneous integration, the unique properties of extreme materials and the opportunities of distributed intelligence will transform our society just as Moore's law has done for the last 50 years.

Bio: Dr. Tomás Palacios is a Professor in the Department of Electrical Engineering and Computer Science at MIT. He received his PhD from the University of California - Santa Barbara in 2006, and his undergraduate degree in Telecommunication Engineering from the Universidad Politécnica de Madrid (Spain). His current research focuses on demonstrating new electronic devices and applications for novel semiconductor materials such as graphene and gallium nitride. His work has been recognized with multiple awards including the Presidential Early Career Award for Scientists and Engineers, the 2012 and 2019 IEEE George Smith Award, and the NSF, ONR, and DARPA Young Faculty Awards, among many others. Prof. Palacios is the founder and director of the MIT MTL Center for Graphene Devices and 2D Systems, as well as the Chief Advisor and co-founder of Cambridge Electronics, Inc. He is a Fellow of IEEE.

BETR Solid State Technology and Devices Seminar

Innovations for Continuation of Moore's Law During Next 10 Years

Tahir Ghani
Intel Senior Fellow
Director, Process Pathfinding Program
Intel Corporation

Friday, May 7, 2021

NOTE: THIS SEMINAR WILL NOT BE RECORDED.

Abstract: Integrated circuit technologies have had a profound impact on the human society during the last 50 years. An early pioneer of integrated circuit age, Gordon Moore projected in 1965 that the transistor density would double every year, which he later modified to doubling every 2 years. An exponential increase in the transistor density during the last 5-decades has continued unabated. As a consequence, the transistor density for the state-of-the-art logic technology is now ~1-2M transistors/mm^2. The enormity of the challenges in maintaining an exponential growth over a period of 5-decades has led many naysayers to periodically announce the impending demise of Moore's Law. However, despite the enormity, these challenges have been surmounted, thanks to the ingenuity of generations of research and development engineers. With the critical dimensions now scaling to sub-10nm regime, there is again an increasing concern that the transistor density has reached close to a plateau. However, I believe that these concerns are again misplaced. In my talk I plan to present new innovations which will enable transistor density to continue to grow during foreseeable future (~10 years). I will describe Gate-all-Around transistor and subsequently a Vertically-Stacked transistor structure, which will serve as the foundation for improving the density and performance/watt metric in future. An increasing role of on-die interconnects, patterning innovations using EUV and novel packaging technologies will serve as effective solutions to improve density and performance at reasonable cost. Finally, I will highlight the ever increasing role of Design-Technology-Co-Optimization (DTCO) towards achieving density and performance improvement beyond pitch reduction. A combination of new transistors, novel interconnects and packaging, EUV patterning, and next generation DTCO tools is expected to enable continuation of Moore's Law into the future, with density reaching ~1B transistors/mm^2.

Bio: Dr. Tahir Ghani is a Senior Fellow and Director of Process Pathfinding Program at Intel Corporation. He received his PhD in Electrical Engineering from Stanford University in 1994. Since joining Intel in 1994, he has led the teams responsible for developing some of the most significant changes in semiconductor industry and implementing them into mainstream CMOS manufacturing. These include uniaxial strained silicon transistors, HiK+Metal Gate transistors and FinFET transistors. He currently leads Intel's Pathfinding Program with focus on technology definition, evaluation of new process innovations and demonstrating their early viability for technologies beyond 2025. His contributions have been recognized by many awards including IEEE Jun-ichi Nishizawa Medal in 2012. He is a Fellow of the IEEE and was elected to the U.S. National Academy of Engineering in 2015.

BETR Solid State Technology and Devices Seminar

Magnonic Spintronics: Toward Spin Wave Based Information Processing

Luqiao Liu
Associate Professor
Department of Electrical Engineering and Computer Science
MIT

Friday, May 14, 2021

Abstract: Spin wave is considered as one of the promising candidates for realizing unconventional computing and interconnection. Compared with other forms of waves, spin wave has many unique features, including short wavelength, intrinsic nonlinearity, non-reciprocity, etc. In this talk I will discuss some of our recent efforts in studying transport properties of spin wave (or equivalently, magnons) in various magnetic structures. In the first example, I will show that there exist mutual interactions between magnons and magnetic domain walls in a ferromagnet, where domain walls change the phase and magnitude of spin waves, and a strong spin wave in turn moves the position of domain walls. This mutual interaction can be used to realize a programmable spin wave phase shifter. In the second example, I will talk about long-range spin transport in an easy-plane antiferromagnet, where the spin angular momentum propagates via the superposition of two linearly polarized magnon modes. We show that the magnon transport in this antiferromagnet can be used to build a non-volatile spin current switch. These mechanisms and device structures could be used as building blocks for future magnon based information processing in the classical and quantum domain.

Bio: Dr. Luqiao Liu is an Associate Professor of Electrical Engineering at Massachusetts Institute of Technology. He received his B.S. in physics from Peking University in 2006, and Ph.D. in Applied Physics from Cornell University in 2012. He worked as a Research Staff Member at IBM Watson Research Center before joining MIT in 2015. Luqiao's current research focuses on spintronic material and devices for memory, logic and communication applications. Luqiao Liu has received the award of McMillan Award, NSF Career Award, Air Force Young Investigator Award, Sloan Fellowship, and International Union of Pure and Applied Physics Young Scientist Award.

Spring 2020 Workshop *Online*

betr
Berkeley Emerging Technologies Research Center

Thursday, June 4, 2020

Zoom link: https://berkeley.zoom.us/j/95035794620

12:00 PM	**Closed Session: Corporate Affiliates and BETR co-Directors**	
	- Opening Remarks	Tsu-Jae King Liu
	- Center Management Updates	Michael Bartl
	- Corporate Affiliates' Dialog with the BETR Center	Jeffrey Bokor (Moderator)
1:00 PM	**Open Session: Welcome**	
1:10 PM	"Silicon Photonics for Sensing and Switching"	Ming Wu
1:30 PM	"Materials innovation for bright and fast LEDs"	Ali Javey
1:50 PM	"Integrated Electronics-Photonics for Sensing, Computing and Communication"	Vladimir Stojanovic
2:10 PM	*Break*	
2:30 PM	**Student & Postdoc Lightning Talks** (3 mins. + 2 mins. Q&A each)	
	"A Fully Integrated Electronic-Photonic Platform for Label-Free Biosensing"	Christos-Georgio Adamopoulos (Stojanovic group)
	"Transfer-Free Fabrication of Atomically Precise Graphene Nanoribbon Field-Effect Transistors"	Zafer Mutlu (Bokor group)
	"Spin-Orbit Torque Generated by Amorphous Fe_xSi_{1-x}"	Jason Hsu (Salahuddin group)
	"A 20x20 Focal Plane Switch Array for Optical Beam Steering"	Xiaosheng Zhang (Wu group)
	"KKY Exchange Coupling Mediated All-Optical Switching of a Ferromagnet"	Jyotirmoy Chatterjee (Bokor group)
	"Error Analysis of Speckle Metrology for an EUV Imaging System"	Gautam Gunjala (Waller group)
	"Physics Can Successfully Implement Lagrange Multiplier Optimization"	Sri Krishna Vadlamani (Yablonovitch group)
	"Wearable Sweat Sensors"	Mallika Bariya (Javey group)
	"Extending the Resolution of Extreme Ultraviolet Lithography with Attenuated Phase-Shift Masks"	Stuart Sherwin (Waller group)
	"Back-End-of-Line Nano-Electro-Mechanical Switches for Reconfigurable Interconnects"	Urmita Sikder (Liu group)
3:20 PM	*Break and switch to Zoom breakout rooms*	
3:30 PM	**Student & Postdoc Virtual Poster Session** *(see below for Zoom breakout room information)*	
4:15 PM	**Closed Session: Feedback – Corporate Affiliates and BETR co-Directors**	

Fall 2020 Workshop *Online*

betr
Berkeley Emerging Technologies Research Center

November 19-20, 2020

Zoom link for November 19: https://berkeley.zoom.us/j/94149082235

November 19, Afternoon

12:00 PM	**Closed Session: Corporate Affiliates and BETR co-Directors**	
	- Opening Remarks	Jeffrey Bokor
	- Center Management Updates	Michael Bartl
	- Corporate Affiliates' Dialog with the BETR Center	Tsu-Jae King Liu (Moderator)
1:00 PM	**Open Session: Welcome**	
1:05 PM	**BETR co-Director Presentations**	
1:10 PM	"Physics-Based Artificial Intelligence"	Eli Yablonovitch
1:30 PM	"Nano-Electro-Mechanical Switches for Future Computing Paradigms"	Tsu-Jae King Liu
1:50 PM	Q&A, Discussion	
2:10 PM	*Break*	
2:25 PM	"New Developments in Ultrafast Spintronics"	Jeffrey Bokor
2:45 PM	"Large Spin Orbit Torque in Amorphous FeSi"	Sayeef Salahuddin
3:05 PM	Q&A, Discussion	
3:25 PM	*Break*	
3:40 PM	**Industry Panel Discussion**	Sayeef Salahuddin (Moderator)
	The New Normal After COVID	
4:50 PM	**Day 1 Wrap-Up**	

Fall 2020 Workshop *Online*

betr
Berkeley Emerging Technologies Research Center

November 19-20, 2020

Zoom link for November 20: https://berkeley.zoom.us/j/97760447291

November 20, Morning

8:00 AM	**Open Session: Welcome**	
8:10 AM	**BETR co-Director Presentations**	
8:10 AM	"Power Sources for Flexible Electronic Devices"	Ana Claudia Arias
8:30 AM	"Computational Microscopy"	Laura Waller
8:50 AM	"Hardware-Software Co-Design for Efficient Machine Learning Execution"	Sophia Shao
9:10 AM	Q&A, Discussion	
9:30 AM	*Break*	
9:50 AM	**Student & Postdoc Lightning Talks**	
	"Bottom-up Graphene Nanoribbon Field-Effect Transistors with High Yield and Performance"	Zafer Mutlu (Bokor group)
	"Enhanced spin-orbit torque in amorphous iron silicon"	Jason Hsu (Salahuddin group)
	"Image Classification with Delay-Based Optoelectronic Reservoir Computing"	Philip Jacobson (Wu group)
	"A Simulation Study of Ultrafast Magnetization Reversal in Spin-Valve Structures"	Debanjan Polley (Bokor group)
	"Printed Miniaturized Batteries for Autonomous Microsystems"	Anju Toor (Arias group)
	"Device-Architecture Co-Optimization of Nonvolatile BEOL NEM Switch Arrays"	Lars Tatum (Liu group)
	"Strain-Tunable Infrared Optoelectronics by Black Phosphorus"	Hyungjin Kim (Javey group)
	"Resonant enhancement of exchange coupling for voltage-controlled magnetic switching"	Shehrin Sayed (Salahuddin group)
	"Picometer Sensitive Metrology for EUV Absorber Phase"	Stuart Sherwin (Waller group)
	"Bioinspired Electronic Skins for Thermosensation and Mechanosensation"	Xiaodong Wu (Arias group)
	"Physics-based Machines for Energy-Efficient Optimization"	Sri Krishna Vadlamani (Yablonovitch group)
10:25 AM	*Break and switch to Zoom breakout rooms*	
10:30 AM	**Student & Postdoc Virtual Poster Session** *(Zoom breakout rooms)*	
11:30 AM	**Closed Session: Feedback – Corporate Affiliates and BETR co-Directors**	
12:00 PM	**Adjournment**	