# betr

Berkeley Emerging Technologies Research Center

# Annual Report

May 2021 – April 2022

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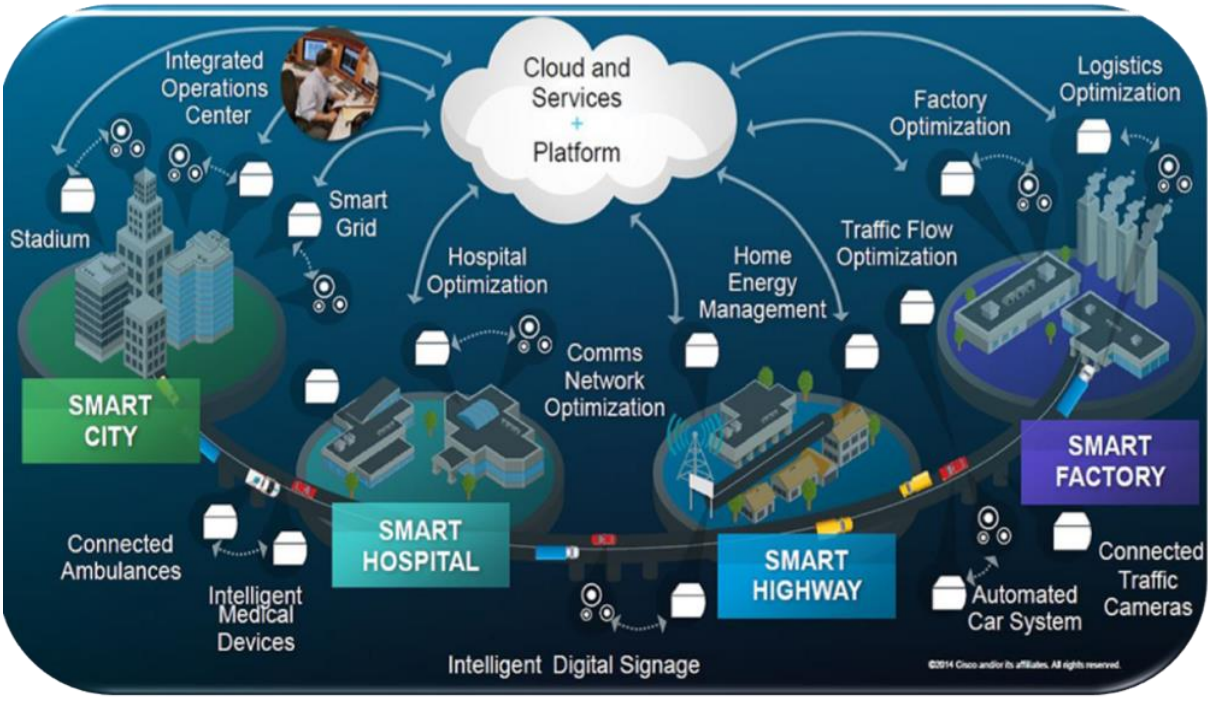
# The Berkeley Emerging Technologies Research Center

## 1.1 Executive Statement

The Berkeley Emerging Technologies Research (BETR) Center is a hub of physical electronics research at the University of California, Berkeley. It serves as a nexus for interactions between faculty and student researchers and leading semiconductor companies for long-term research collaborations and knowledge transfer. Research activities in the BETR Center encompass a wide range from the search for new materials and manufacturing processes to the development of novel computing and memory devices and the design of heterogeneous integrated systems.

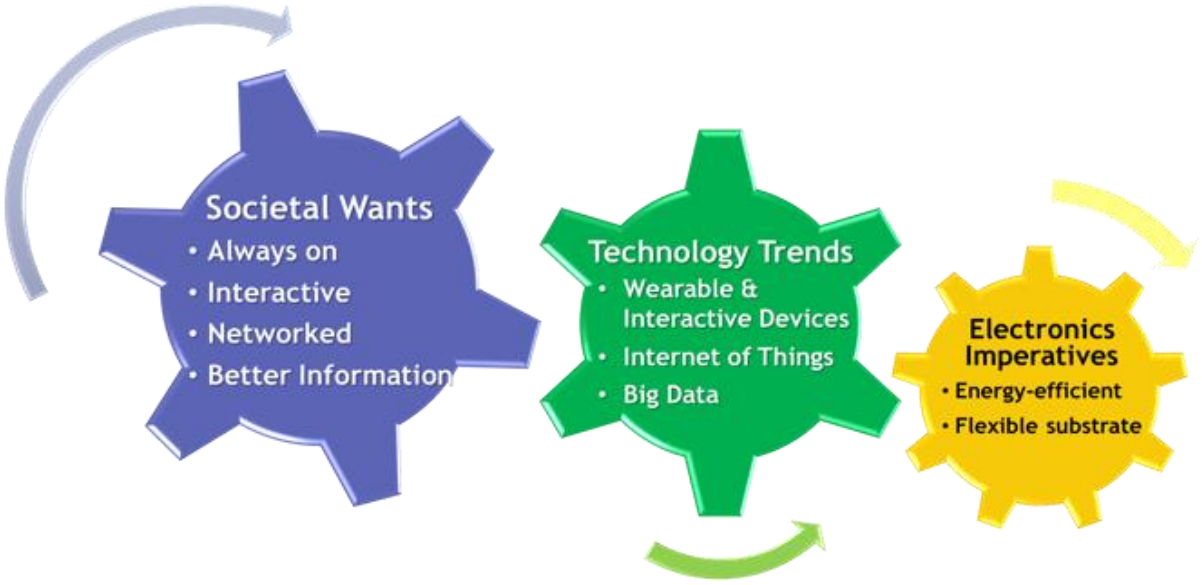
**The mission of the BETR Center is to foster innovation in materials, processes and devices toward the vision of ubiquitous information systems for enhancing health and quality of life in our global society.**

For the last five decades, steady miniaturization of the transistor has yielded continual improvements in integrated-circuit performance and cost per function, with dramatic impact on virtually every aspect of life in modern society. This proliferation of information and communication technologies has enabled cloud computing and the Internet of Things, which together with recent advancements in machine learning give rise to the vision of an *artificially intelligent world* with systems for coordinating critical infrastructure for *smart cities*, managing personalized health care and medicine for *smart hospitals*, automating vehicles and traffic flow for *smart highways*, and optimizing manufacturing and logistics for *smart factories*.



The real-time processing of large quantities of data required by artificially intelligent systems is possible today because of the dramatic improvement of the capabilities of computing devices. This exponential increase of computation power in the last 120 years is described in Kurzweil's Law, which predicts that computing systems are rapidly approaching the capability of the human brain. Underlying Kurzweil's Law is Moore's Law, describing the evolution of transistors fueled by advancements in materials, processes, and structures that have enabled transistors to be miniaturized to sub-20 nm feature sizes in the most advanced chips today. However, as fundamental limits are approached, transistor scaling will not be as straightforward in the future as it has been in the past. Alternative approaches for improving chip functionality, cost per function and energy efficiency eventually will thus be necessary to sustain the rapid growth of the semiconductor industry beyond the next decade.

The BETR Center is ideally positioned to address these challenges by bringing together a broad range of world-renowned leaders in electronic devices and technology research. The BETR team of UC Berkeley professors, postdocs, and students collaborates across the disciplines of electrical engineering, computer science and materials science to build the technological foundation for future ubiquitous information systems. Considering that artificially intelligent systems must always be awake, interactive, and networked across many devices, it is imperative that future electronic systems are more energy efficient in order to be ubiquitous, and they need to be compatible with flexible substrates to be wearable.




## 1.2 Leadership Team

To meet the need for a new industry growth paradigm (beyond Moore's Law), the BETR Center brings together research leaders whose collective expertise spans not only materials, structures and manufacturing processes for nanoelectronics, nanomagnetics, nanophotonics and optoelectronics

but also computational imaging and metrology, and IC design and system architecture. In fact, BETR faculty co-directors have contributed significant innovations to sustain Moore's Law in the last few decades, including the development of "spacer lithography" (also known as self-aligned double patterning, SADP) for patterning of sub-lithographic features, the "FinFET" (a fin-shaped field-effect transistor structure) for transistor scaling to below 10 nm, and most recently the "negative capacitance FET" to reduce transistor operating voltage.

***Faculty co-Directors*** *(in alphabetical order)*

### Ana Claudia Arias

Printed and Flexible Electronics

Dr. Ana Claudia Arias is a professor in the Department of Electrical Engineering and Computer Science at UC Berkeley. She received her Ph.D. in Physics from the University of Cambridge, UK in 2001. Prior to that, she received her master's and bachelor's degrees in physics from the Federal University of Paraná in Curitiba, Brazil in 1997 and 1995, respectively.

Dr. Arias joined the University of California, Berkeley in January of 2011. Before that she was manager of the Printed Electronic Devices Area and a Member of Research Staff at PARC, a Xerox Company. She went to PARC, in 2003, from Plastic Logic in Cambridge, UK where she led the semiconductor group. Her research focuses on the use of electronic materials processed from solution in flexible electronic systems. Dr. Arias uses printing techniques to fabricate flexible large area electronic devices and sensors.

### Jeffrey Bokor

Embedded Memory, Millivolt Switches, Integrated Systems

Dr. Jeffrey Bokor is the Paul R. Gray Distinguished Professor of Engineering in the Department of Electrical Engineering and Computer Sciences at UC Berkeley, with a joint appointment as Senior Scientist in the Materials Science Division at Lawrence Berkeley National Laboratory.

Dr. Bokor received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology in 1975, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1976 and 1980, respectively. From 1980 to 1993, he was at AT&T Bell Laboratories where he did research on a variety of topics in laser science, advanced lithography for integrated circuits, as well as semiconductor physics and technology, and held several management positions.

Dr. Bokor joined the Berkeley faculty in 1993 and served in a number of administrative positions including Associate Dean for Research in the College of Engineering, and Chair of the Electrical Engineering and Computer Science Department. His current research activities include nanomagnetics/spintronics, graphene electronics, nanophotonics, and nano-electromechanical systems. He is a fellow of IEEE, APS, and OSA.

### Ali Javey

Flexible Electronics, Millivolt Switches

Dr. Ali Javey is the Lam Research Distinguished Chair in Semiconductor Processing and a professor of Electrical Engineering and Computer Sciences at UC Berkeley. He is also a senior faculty scientist at the Lawrence Berkeley National Laboratory where he serves as the program leader of Electronic Materials (E-Mat). He is a co-director of Berkeley Sensor and Actuator Center (BSAC) and an associate editor of ACS Nano.

Dr. Javey received a Ph.D. degree in chemistry from Stanford University in 2005 and was a Junior Fellow of the Harvard Society of Fellows from 2005 to 2006 before joining the faculty at UC Berkeley. His research interests encompass the fields of chemistry, materials science, and electrical engineering and focus on the integration of nanoscale electronic materials for various technological applications, including low power electronics, flexible circuits and sensors, and energy generation and harvesting.

Dr. Javey is the recipient of numerous awards, including the Dan Maydan Prize in Nanoscience Research, the MRS Outstanding Young Investigator Award, the Nano Letters Young Investigator Lectureship, the National Academy of Sciences Award for Initiatives in Research, Technology Review TR35, and the NSF Early CAREER Award.

### Tsu-Jae King Liu

Millivolt Switches, Embedded Memory, Integrated Systems

Dr. Tsu-Jae King Liu is the Dean of the College of Engineering and the Roy W. Carlson Professor of Engineering at UC Berkeley. Previously, she served as Chair of the EECS Department, Associate Dean for Research in the College of Engineering, and Faculty Director of the Marvell Nanofabrication Laboratory. She was also Senior Director of Engineering in the Advanced Technology Group of Synopsys, Inc. (2004-2006).

She received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from Stanford University. She joined the Xerox Palo Alto Research Center as a Member of Research Staff in 1992, to research and develop high-performance thin-film transistor technologies for flat-panel display applications. In 1996 she joined the faculty at UC Berkeley. Her research activities are presently in advanced materials, fabrication processes and devices for energy-efficient electronics. She has authored or co-authored over 550 publications and holds over 95 patents.

Dr. Liu's awards include the DARPA Significant Technical Achievement Award for development of the FinFET, the IEEE Kiyo Tomiyasu Award, the Intel Outstanding Researcher in Nanotechnology Award, and the Semiconductor Research Corporation (SRC) Aristotle Award. Dr. Liu is a Fellow of the IEEE and a member of the U.S. National Academy of Engineering, and she serves on the Board of Directors for Intel Corporation and on the Board of Directors for MaxLinear, Inc.

## Ramamoorthy Ramesh

Spin-Based Logic, Embedded Memory, Multiferroics

Dr. Ramesh is the Purnendu Chatterjee Chair Professor in Materials Science and Physics at UC Berkeley, and a Faculty Senior Scientist at Lawrence Berkeley National Laboratory. He pursues key materials physics and technological problems in complex multifunctional oxides. Using conducting oxides, he solved the 30-year enigma of polarization fatigue in ferroelectrics. He pioneered research into manganites coining the term, Colossal Magnetoresistive (CMR) Oxides. His work on multiferroics demonstrated electric field control of ferromagnetism, a critical step towards ultralow power memory and logic elements. His extensive publications on the synthesis and materials physics of complex oxides are highly cited (over 98,000 citations, H-factor =151).

He is a fellow of APS, AAAS & MRS and an elected member of the U.S. National Academy of Engineering and a Foreign member of the Royal Society of London. His awards include the Humboldt Senior Scientist Prize, the APS Adler Lectureship and McGroddy New Materials Prize, the TMS Bardeen Prize and the IUPAP Magnetism Prize and Neel Medal. He was recognized as a Thomson-Reuters Citation Laureate in Physics for his work on multiferroics.

He served as the Founding Director of the successful Department of Energy SunShot Initiative in the Obama administration, envisioning and coordinating the R&D funding of the U.S. Solar Program, spearheading the reduction in the cost of Solar Energy. He also served as the Deputy Director of Oak Ridge National Laboratory and the Associate Lab Director at LBNL.

## Sayeef Salahuddin

Embedded Memory, Accelerators for AI, Millivolt Switches

Dr. Sayeef Salahuddin is the TSMC Distinguished Professor of Electrical Engineering and Computer Sciences at UC Berkeley. He is the co-director of the Berkeley Center for Negative Capacitance Transistors (BCNCT) and the Berkeley Device Modeling Center (BDMC), and he is an associate director of ASCENT, a multi-university research center within the DARPA/SRC JUMP initiative.

His research lab explores the conceptualization and demonstration of novel device physics for logic and memory applications. Dr. Salahuddin is widely known for his discovery of the Negative Capacitance phenomenon in ferroelectric materials.

Dr. Salahuddin has received the Presidential Early Career Award for Scientist and Engineers (PECASE), the highest honor bestowed by the US Government on early career scientists and engineers. He also received a number of other awards including the NSF CAREER award, the IEEE Nanotechnology Early Career Award, the Young Investigator Awards from the AFOSR and ARO and the IEEE George Smith Award. He is a Fellow of the IEEE and the APS.

### Sophia Shao

Accelerators for AI, Integrated Systems

Dr. Sophia Shao is an Assistant Professor and an SK Hynix Faculty Fellow in the Electrical Engineering and Computer Sciences department at UC Berkeley. Previously, she was a Senior Research Scientist at NVIDIA Research.

Dr. Shao received her Ph.D. degree in 2016 and S.M. degree in 2014 from Harvard University. Her research interests are in the area of computer architecture, with a special focus on specialized accelerator, heterogeneous architecture, and agile VLSI design methodology.

Dr. Shao's work has been awarded a Best Paper Award (MICRO 2019) and Top Picks in Computer Architecture (2014). Her Ph.D. dissertation was nominated by Harvard for ACM Doctoral Dissertation Award. Dr. Shao is a Siebel Scholar, an invited participant at the Rising Stars in Electrical Engineering and Computer Science Workshop, and a recipient of the IBM Ph.D. Fellowship.

### Vladimir Stojanović

Accelerators for AI, Optical Interconnects, Integrated Systems

Dr. Vladimir Stojanović is Professor of Electrical Engineering and Computer Science at UC Berkeley. He received his Ph.D. in Electrical Engineering from Stanford University in 2005, and the Dipl. Ing. degree from the University of Belgrade, Serbia in 1998. He was also with Rambus, Inc., Los Altos, CA, from 2001 through 2004 and with MIT as Associate Professor from 2005 to 2013.

Research interests of Dr. Stojanović include design, modeling and optimization of integrated systems, from CMOS-based VLSI blocks and interfaces to system design with emerging devices like NEM relays and silicon-photonics. He is also interested in design and implementation of energy-efficient electrical and optical networks, and digital communication techniques in high-speed interfaces and high-speed mixed-signal IC design.

Dr. Stojanović received the IBM Faculty Partnership Award, the NSF CAREER Award, the ICCAD William J. McCalla, the IEEE Transactions on Advanced Packaging, and the ISSCC Jack Raper best paper award. He was an IEEE Solid-State Circuits Society Distinguished Lecturer for the 2012-2013 term.

## Laura Waller

Computational Microscopy

Dr. Laura Waller is an Associate Professor of Electrical Engineering and Computer Science at UC Berkeley, leading the Computational Imaging Lab. She is a Senior Fellow at the Berkeley Institute of Data Science (BIDS), with affiliations in Bioengineering and Applied Sciences & Technology. From 2016 to 2020 Dr. Waller held the UC Berkeley Ted Van Duzer Endowed Professorship.

Dr. Waller was a Postdoctoral Researcher and Lecturer of Physics at Princeton University from 2010-2012 and received B.S., M.Eng. and Ph.D. degrees from Massachusetts Institute of Technology in 2004, 2005 and 2010, respectively. She is a Moore Foundation Data-Driven Investigator, Bakar fellow, Distinguished Graduate Student Mentoring awardee, NSF CAREER awardee, Chan-Zuckerberg Biohub Investigator, SPIE Early Career Achievement Awardee and Packard Fellow.

## Ming C. Wu

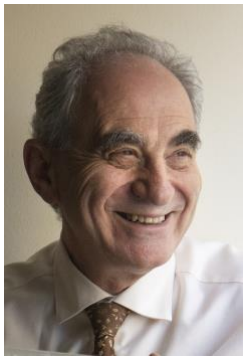
Photonics, Optical Interconnects, Accelerators for AI

Dr. Ming C. Wu is Nortel Distinguished Professor of Electrical Engineering and Computer Sciences and Co-Director of the Berkeley Sensor and Actuator Center (BSAC) and the Berkeley Emerging Technologies Research (BETR) Center at UC Berkeley. Dr. Wu received his B.S. degree in Electrical Engineering from National Taiwan University in 1983, and M.S. and Ph.D. degrees in Electrical Engineering and Computer Sciences from the University of California, Berkeley in 1986 and 1988, respectively.

From 1988 to 1992, he was Member of Technical Staff at AT&T Bell Laboratories, Murray Hill, New Jersey. From 1992 to 2004, he was Professor of Electrical Engineering at the University of California, Los Angeles (UCLA). He has been a faculty member at Berkeley since 2004.

His research interests include silicon photonics, optoelectronics, MEMS, MOEMS, and optofluidics. He has published 8 book chapters, over 600 papers in journals and conferences, holds 30 U.S. patents. His research has been successfully commercialized by OMM (MEMS optical switches, 1997) and Berkeley Lights (NASDAQ:BLI, optofluidics, 2011).

Prof. Wu is Fellow of IEEE and Optical Society (OSA), and a Packard Foundation Fellow (1992 – 1997). He was a member of the IEEE Photonics Society Board of Governors from 2013 to 2016. His work has been recognized by the 2016 IEEE Photonics Society William Streifer Scientific Achievement Award, the 2007 Paul F. Forman Engineering Excellence Award, the 2017 C.E.K. Mees Medal from the Optical Society (OSA), and the 2020 Robert Bosch Micro and Nano Electro Mechanical Systems Award from IEEE Electron Device Society.



**Eli Yablonovitch**

Millivolt Switches, Photonics, Accelerators for AI

Dr. Eli Yablonovitch holds the James & Katherine Lau Chair in Engineering in the Department of Electrical Engineering and Computer Sciences at UC Berkeley. Dr. Yablonovitch received his Ph.D. degree in Applied Physics from Harvard University in 1972. He worked for two years at Bell Telephone Laboratories, and then became a professor of Applied Physics at Harvard. He joined Exxon in 1979 and Bell Communications Research in 1984, before joining UCLA in 1992. Since 2007 he is a faculty member at UC Berkeley.

Prof. Yablonovitch introduced the idea that strained semiconductor lasers could have superior performance due to reduced valence band (hole) effective mass. With almost every human interaction with the internet, optical telecommunication occurs by strained semiconductor lasers. He is regarded as a Father of the Photonic BandGap concept, and he coined the term "Photonic Crystal". The geometrical structure of the first experimentally realized Photonic bandgap, is sometimes called "Yablonovite". In his photovoltaic research, Prof. Yablonovitch introduced the 4(n squared) ("Yablonovitch Limit") light-trapping factor that is in worldwide use, for almost all commercial solar panels. His mantra that "a great solar cell also needs to be a great LED", is the basis of the world record solar cells: single-junction 29.1% efficiency; dual-junction 31.5%; quadruple-junction 38.8% efficiency; all at 1 sun. Dr. Yablonovitch is elected as a Member of the National Academy of Engineering, the National Academy of Sciences, the National Academy of Inventors, the American Academy of Arts & Sciences, and is a Foreign Member of the Royal Society of London.

### *Executive Director*

**Michael H. Bartl**

Center Administration

Dr. Michael H. Bartl is the executive director of the Berkeley Emerging Technology Research (BETR) Center and, until March 2022, he also served as executive director of the NSF Science & Technology Center for Energy Efficient Electronics Science ($E^3S$). Before moving to Berkeley, Dr. Bartl was a tenured faculty member at the University of Utah (where he still holds an appointment as research professor), and a visiting professor at the Technical University of Munich, Germany. He co-founded Navillum Nanotechnologies and published more than 65 papers about his research activities in functional nanostructured materials for energy and information technology applications.

A native of Austria, Dr. Bartl earned his doctorate in chemistry from Karl-Franzens University Graz before conducting postdoctoral research at the UC Santa Barbara. He was the recipient of a "DuPont Young Professorship", and he was named a Scialog Fellow by the Research Corporation for Science Advancement and a "Brilliant 10" researcher by Popular Science magazine.

## 1.3 Corporate Membership

The BETR Center was established with the goal to foster long-term academia-industry research collaborations and knowledge transfer by connecting UC Berkeley faculty and students who are building the technological foundation for future electronic devices and information systems with leading semiconductor companies. The BETR Center model of mutually beneficial collaborations gives corporate members early access to innovative ideas and research results, while university researchers gain insights into technological challenges faced by industry and society, and by seeing the results of their research applied to solve real-world problems. Moreover, the BETR Center provides various opportunities for member companies to interact directly with its faculty co-directors and 100+ graduate students and postdocs, many of whom are prospective future employees.


Since its inception in 2016, the BETR Center has seen a steady increase in the number of corporate members, and we are delighted to currently have eight leading companies in innovation in the semiconductor industry be part of the BETR Center. These companies are (in alphabetical order): AMD, Applied Materials, Atomera, Intel Corporation, Lam Research, Meta (formerly Facebook), SK Hynix, and TSMC.

Each of the member companies is represented in the BETR Center Technical Advisory Board (TAB). The TAB meets biannually as part of the BETR Center Workshops in a closed session to promote dialog between industry and academia. As such, the TAB is a crucial body in providing all BETR faculty co-directors important feedback for on-going research and future directions.

Moreover, since the TAB comprises members from across the industrial ecosystem, it provides BETR Center researchers with multiple and holistic perspectives. Additional benefits of a BETR Center corporate membership include:

### Access to Periodic Research Webinars

During the fall and spring semesters, the BETR Center hosts a series of webinars featuring leading-edge research within the fields of physical electronics and optoelectronics. Given by researchers from UC Berkeley and other research institutions, these webinars are accessible via an online meeting service. Recordings of most of these webinars are made available to corporate members via password-protected access on the BETR website. In the 2021/22 reporting period, the BETR Center hosted and shared 21 webinars (see Appendix A for details).

### Attendance at Semi-Annual Research Reviews/Workshops

The BETR Center holds two research reviews/workshops per year in which the latest research results are presented. These events include oral presentations, industry panels, and lightning talks and poster sessions by BETR students and postdocs, offering an opportunity to meet and interact with student presenters, who are potential candidates for internships and/or employment. In 2021, two BETR Workshops were held (agendas for the spring and fall workshops are given as Appendix B and Appendix C, respectively).

### Invitation to Berkeley EECS Annual Research Symposium (BEARS)

Each year in February, UC Berkeley's Department of Electrical Engineering and Computer Sciences hosts a day-long research conference featuring a variety of informative talks by distinguished faculty members and advanced graduate students. BEARS gives industrial affiliates a look at some of the most exciting research being pursued in information science and technology.

### Customized Briefings

Upon request, the BETR Center staff will facilitate the scheduling of meetings with individual BETR Center co-directors. Based on best efforts, they will also facilitate introductions to other research centers and programs at UC Berkeley, as well as to companies that are part of UC Berkeley's technology innovation ecosystem.

### Option to Direct Part of the Membership Contribution to a Faculty co-Director

Each corporate affiliate may direct part of the monetary membership contribution to specific research project(s) or research team(s). Typically, this is request is made at the start of the annual membership period. The BETR Center co-directors will then review requests and endeavor to allocate part of the contribution to support those research topics. Acknowledgment of the company's support will be made in all publication of the results from studies that are funded specifically by the allocated portion of the company's gift.

### Facilitation of Technology Licensing

Twice a year, a list of research publications and patent applications will be provided to all industry affiliates. Upon request, the BETR Center staff will facilitate introductions to the Industry Alliances Office and Office of Technology Licensing at UC Berkeley for technology licensing.

# 2 Research Activities

## 2.1 Motivation and Overview

The central goal of the BETR Center is to provide solutions for driving innovation in materials, processes and solid-state devices to enable future ubiquitous information systems. Research activities are motivated by three main challenges for *ambient intelligence* to become a reality:

**Looming Power Crisis for Computing:** Electricity consumed by computing devices has increased exponentially with the proliferation of information and communication technology. To avoid a power crisis in the future, fundamentally new concepts for more energy-efficient logic switches and on-chip communication are needed. In addition to breakthroughs in solid-state science and technology, innovations in circuit design and system architecture will be necessary to avert a power crisis for computing.

**Advent of the Internet of Things:** The Internet of Things era of ubiquitous computing, wherein electronic devices are pervasive and wirelessly networked with access to cloud computing requires heterogeneous integration to diversify functionality and mechanical flexibility in mobile devices. For these to be affordable, new manufacturing techniques must be developed through interdisciplinary research into novel tools, processes, and materials that are compatible with low-cost plastic substrates.

**Proliferation of Big Data Applications:** "Big Data" has become the main driver for advances in memory technology and high-performance computing with increasing need for storing and processing large data sets in real-time to derive actionable information. Hardware innovations (including non-von-Neumann architectures) and new computational algorithms and software systems will be needed to meet the demand within reasonable energy and cost constraints.

Finding solutions to these grand challenges requires a concerted effort across disciplines and between academic and industrial researchers. In response, the BETR Center assembled a diverse group of UC Berkeley professors from electrical engineering, computer science and materials science, working with industry researchers, to build the technological foundation for future electronic devices and information systems. The BETR Center research teams are organized in six distinct, but highly collaborative, research thrusts (Figure 1): (1) Next-Generation Devices (including Millivolt Switches and Embedded Memory), (2) Flexible Electronics, (3) Accelerators for AI, (4) System Integration, (5) Optical Interconnects, (6) Metrology. In the following, information for each of the research thrusts is provided, including key achievements in the last twelve months and a description of current and future projects.

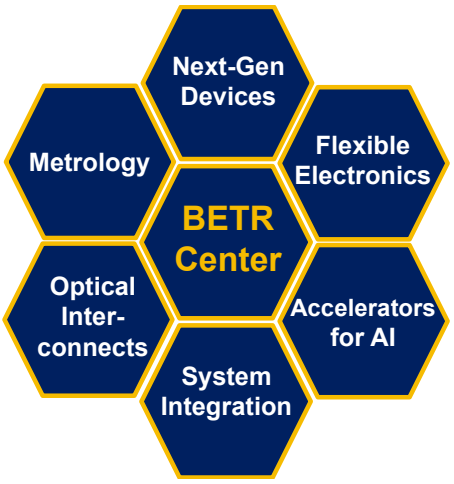



**Figure 1.** Research Thrusts of the BETR Center.

## 2.2 Millivolt Switches

*Research activities of the Millivolt Switches Thrust have been supported in part by directed membership contributions of **TSMC**, **SK Hynix**, **Intel Corporation**, and **Atomera**.*

Energy-efficient electronic devices are central to the BETR Center's research mission. Given recent advancements in cloud computing, social networking, mobile internet and data analytics, and the associated increase of battery-powered electronic systems, the development of intelligent systems that can operate at significantly reduced power consumption is now as relevant as ever. In fact, many of the ultra-low power electronics research projects in the BETR Center have originated in the Center for Energy Efficient Electronics Science ($E^3S$) based on the recognition that the energy used to manipulate a single bit of information is currently ~100,000 times greater than the theoretical limit. Research on ultra-low power devices and circuits in the BETR Center is conducted by **Professors Jeffrey Bokor**, **Ali Javey**, **Tsu-Jae King Liu**, **Sayeef Salahuddin**, and **Eli Yablonovitch**, and encompasses the search for alternatives to classical transistor-based digital logic. Examples include new circuit and system architectures leveraging zero-leakage nano-electromechanical (NEM) relays, field effect transistors (FETs) with 2D materials as active layers, and graphene nanoribbon transistors.[MS1-MS4]

### 2.2.1 Recent Achievements

#### *A. Graphene Nanoribbons*

Research on graphene nanoribbon (GNR) based millivolt switches in the BETR Center is led by the **Bokor** group (and Prof. Felix Fischer), in collaboration with BETR industry affiliate **TSMC**. The BETR team has successfully synthesized several distinct GNRs with ultra-narrow width (0.7-3.0 nm), atomically smooth edges and uniform bandgap. Furthermore, as shown in Figure 2 (left), fabrication processes were developed to integrate GNRs into functioning FETs with excellent switching behavior (ON/OFF ratios of ~$10^5$ and ON-currents ($I_{on}$) of ~60 nA).[MS3,MS5] However, since the bottom-up synthesis commonly takes place on catalytic metallic surfaces, the integration of GNRs into such devices requires their transfer onto insulating substrates, which remains one of the bottlenecks in the development of GNR-based electronics. In response, the **Bokor** group developed a method for the transfer-free placement of GNRs on insulators, involving growth of GNRs on a gold film deposited onto an insulating layer followed by gentle wet etching of the gold, which leaves the nanoribbons to settle in place on the underlying insulating substrate (Figure 2, right).[MS5] Meanwhile, the team has also demonstrated

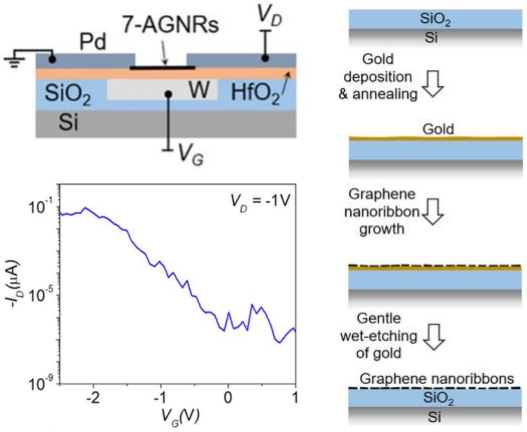



**Figure 2. Left.** Schematic representation (top) and $I_D$–$V_G$ characteristics (bottom) of 7-AGNR FETs with Pd source–drain electrodes and local $HfO_2$ back gate. **Right.** Schematic of the transfer-free synthesis of GNRs on $SiO_2$/Si substrates. Typical AFM height images of a ~100 nm gold thin film deposited onto a $SiO_2$/Si substrate.

transfer-free fabrication of ultrashort channel GNR FETs using this process. Importantly, this process can scale up well to 12-inch wafers, which is extremely difficult for previous techniques.

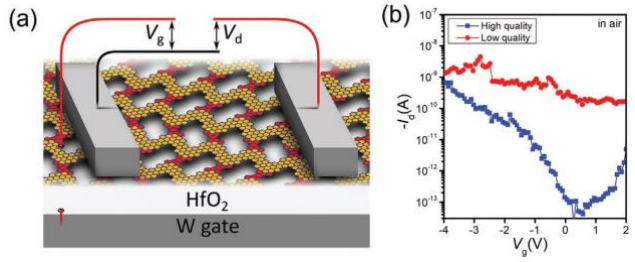



**Figure 3. a)** Schematic of the device structure of a local back-gated chevron NPG FET. **b)** Room temperature $I_d$–$V_g$ characteristics of the FET devices prepared from the high-quality and low-quality chevron NPG samples measured at $V_d$ = −2 V in air.

In a parallel approach, the BETR team has demonstrated a new bottom-up fabrication method for nanoporous graphene (NPG) short-channel FETs with excellent properties.[MS4] In detail, FETs based on bottom-up synthesized chevron-type NPG, consisting of ordered arrays of nanopores defined by laterally connected chevron GNRs were demonstrated (Figure 3a). The devices displayed excellent switching behavior with ON-OFF ratios exceeding $10^4$ (Figure 3b) which makes them potentially promising for logic applications. This new method shows that bottom-up fabrication gives access to a superior NPG material due to control over the geometry and electronic properties at the atomic level.

In collaboration with researchers from MIT, the **Bokor** group achieved ohmic contact between semi-metallic bismuth and semiconducting monolayer.[MS6] The group reported a zero Schottky barrier height, a record-low contact resistance of 123 ohm micrometers, and a record-high on-state current density of 1,135 microamps per micrometer. It should be emphasized that the reported contact resistances approach the quantum limit for two-dimensional semiconductors. The team also demonstrated that this approach for forming ohmic contacts can be extended to a range of monolayer semiconductors, including $MoS_2$, $WS_2$ and $WSe_2$. This technology unveils the potential of high-performance monolayer transistors that are on par with state-of-the-art three-dimensional semiconductors, enabling further device downscaling and extending Moore's law.

### *B. Low-Temperature Semiconductor Processing*

Processing of high-quality semiconductors at near-ambient temperatures has become increasingly important for both transparent/flexible electronics and monolithic 3D-CMOS architectures. While several solutions exist for n-type semiconductors, the **Javey** group recently reported a breakthrough for p-type semiconductors by successful thermal evaporation of tellurium thin films at cryogenic temperatures.[MS7] In this period, the group performed in-depth

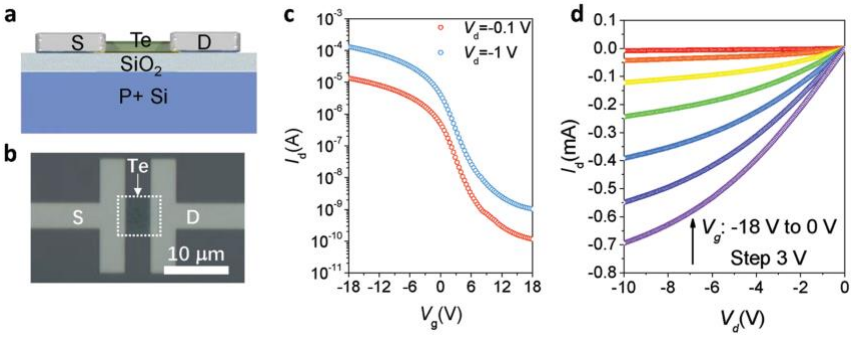



**Figure 3.** Field-effect transistors based on Te films crystallized at different temperatures. a) Schematic diagram of the device structure. b) Optical image of a typical FET based on the single grain Te film crystallized at 5°C. c) $I_d$–$V_g$ transfer curves, d) $I_d$–$V_d$ output characteristics.

studies on the kinetics and dynamics of the crystallization of thermally evaporated Te films by visualization and modeling.[MS8] Low-temperature processing of highly crystalline tellurium films with large grain size and preferred out-of-plane orientation (i.e., (100) plane parallel to the surface) was demonstrated by controlling the crystallization process. Using this approach, the team grew tellurium single crystals with a lateral dimension of up to 6 μm on various substrates including glass and plastic.

Field effect transistors (FETs) were fabricated using Te films as the channel, and $SiO_2$ (50 nm thick)/p+-Si as dielectric layer and back-gate to examine the electronic properties of low-temperature crystallized Te, as shown in Figure 3a and 3b. The fabricated FETs exhibited a typical p-type characteristic due to native defects (Figure 3c) with remarkable subthreshold swing of 2.7 V $dec^{-1}$. Moreover, excellent effective hole mobility of 93 $cm^2$ $V^{-1}$ $s^{-1}$ and ON/OFF current ratios of $\approx 10^5$ were observed at room temperature in vacuum environment. Various functional logic gates and circuits were demonstrated by integrating multi-layered transistors on a single chip using sequential lithography, deposition and lift-off processes.[MS7]

### *C. Novel Switches Based on NEM Relays and Inserted-Oxide FinFETs*

The **Liu** group has pioneered the use of non-volatile nano-electromechanical (NEM) switches (or relays) for energy efficient computing.[MS9] NEM switches use electrostatic force to mechanically actuate a movable structure to make or break physical contact between current-conducting electrodes. Importantly, when the electrodes are separated physically by an air gap, no current flows across the gap, resulting in zero OFF-state current. Hence NEM switches have abrupt ON/OFF switching characteristics, in addition to robust operation across a wide temperature range, down to cryogenic temperatures.[MS10] Recent work by the **Liu** group demonstrated that non-volatile NEM switches can be monolithically integrated with CMOS circuitry, using multiple metallic layers in the BEOL stack of a standard 65nm CMOS process, followed by a release etch after CMOS fabrication.[MS11] In this period, the **Liu** group projected that optimally designed non-volatile NEM switches implemented with three BEOL layers in a 5-nm CMOS technology can be programmed with CMOS-compatible voltages and are expected to be more compact than SRAM cells and much more energy-efficient (with sub 5-aJ write energy) than any other type of non-volatile memory device.[MS12]

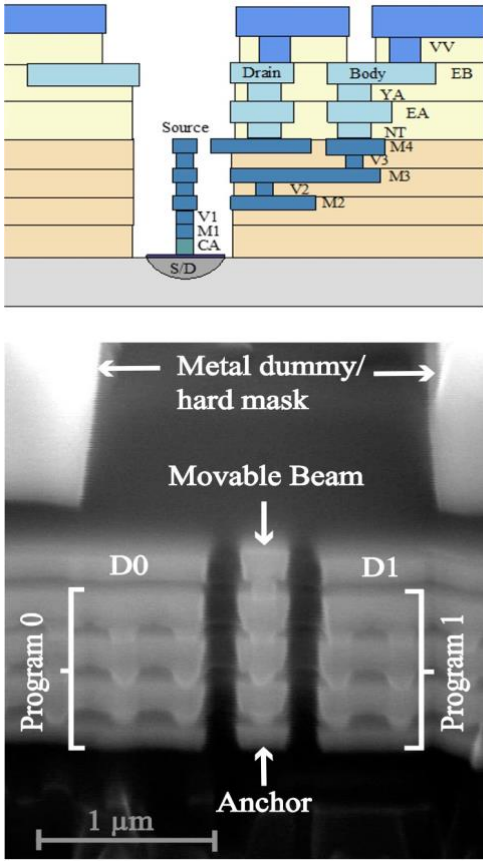



**Figure 4.** Schematic cross-section view (**top**) and SEM image (**bottom**) of a vertical NEM switch fabricated using multiple layers in a standard BEOL process in 65nm CMOS technology.

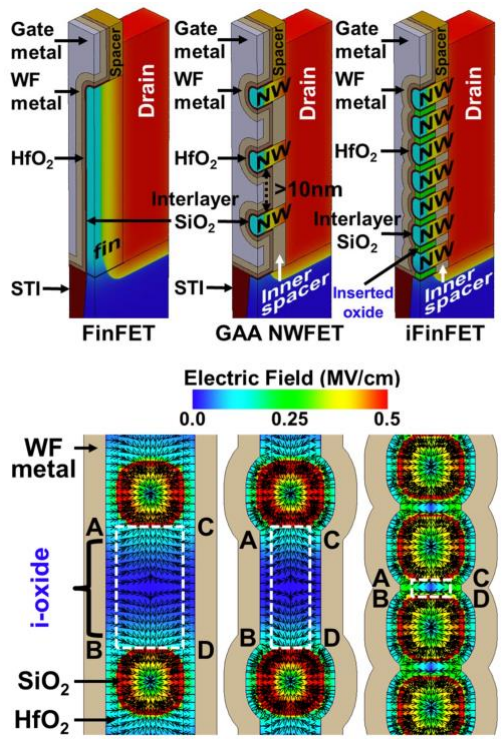



**Figure 5.** Double-cutaway views (**top**) and turned-on state electric field distribution (**bottom**) of a FinFET, a GAA 3- NWFET, and a 7-NW iFinFET. **Top.** The colors indicate the net dopant concentration profiles, as simulated by Synopsys Sentaurus software. **Bottom.** ABCD denote four corners of the i-oxide. For simplicity, only a portion of NWs are shown, and the gate metal layers are not depicted.

The **Liu** group also introduced a new high-permittivity (high-k) inserted-oxide FinFET (iFinFET) structure with low-permittivity inner spacers for CMOS transistor scaling to the 3-nm technology node and beyond (Figure 5, top).[MS13] The process to fabricate an iFinFET is similar to fabricating a nanosheet field-effect transistor (NSFET) and no additional lithography masks are needed. Importantly, the proposed iFinFET requires only a single ultrathin high-k inserted-oxide (i-oxide) layer between the nanowires, allowing more nanowires to be vertically stacked within the constraint of a maximum total channel height. This is in strong contrast to the NSFET and to the nanowire field effect transistor (NWFET), which each require significant spacing between the nanosheets or nanowires to accommodate metallic gate and dielectric insulator multilayer stacks (Figure 5, bottom). The i-oxide layers of the iFinFET allow fringing electric fields from the gate to penetrate into the NWs to achieve improved electrostatic integrity. When comparing simulated performance characteristics of the proposed iFinFET device structure against those for the FinFET, NWFET, and NSFET, the iFinFET is projected to provide superior electrical performance when the footprint (device layout width) is less than 80 nm.

## 2.2.2 Current Projects

### Graphene Nanoribbon-Based Millivolt Switches

*(Prof. Jeffrey Bokor)*

In collaboration with UC Berkeley synthetic chemist Prof. Felix Fischer, this project focusses on the synthesis of novel graphene nanoribbons (GNRs) and their integration into functioning field effect transistor (FET) devices. Recently, they demonstrated the excellent switching behavior of GNR-based FETs with ON/OFF ratios of ~$10^5$ and ON-currents ($I_{on}$) of ~60 nA.[MS3] Current work aims at upscaling GNR FET fabrication using a transfer-free placement of GNRs on insulators.[MS5] While the concept has been successfully demonstrated, the device performance was lower than with previous processes. The main focus now is to optimize this new transfer-free placement of GNRs process to increase both ON/OFF ratios and ON-currents. Since the transfer-free process can scale up well to 12-inch wafers, it is an important step toward large-scale integration of GNRs into electronic devices.

**NEM Switches Monolithically Integrated with CMOS Circuitry**

*(Prof. Tsu-Jae King Liu)*

Nanoelectromechanical (NEM) switches can be operated at ultralow voltages (<20 mV) and have abrupt ON/OFF switching characteristics, in addition to robust operation across a wide temperature range. Taking advantage of ultra-scaled interconnect pitch in state-of-the-art CMOS technology, the team demonstrated that vertical non-volatile NEM switches can be implemented using multiple interconnect layers in the back-end-of-line (BEOL) stack of a standard 65nm CMOS process.[MS10-MS12] Such integrated systems have enormous potential for CMOS power gating, configuration of field-programmable gate arrays, non-volatile back-up storage of information in SRAM and CAM cells, and energy-efficient, fast and reconfigurable look-up tables. With support of BETR industry affiliate **SK Hynix**, the current project focuses on demonstration of BEOL NEM switches at extreme temperature conditions and on technology scaling to achieve programming voltage of NEM switches in the range compatible with standard I/O CMOS circuitry. A significant step in this direction has recently been achieved by demonstrating functional vertical non-volatile NEM switches and hybrid reconfigurable circuits in TMSC's 16nm FinFET CMOS process.

**Monolithic 3D CMOS**

*(Prof. Ali Javey)*

The Javey group has been exploring new materials and process schemes to enable synthesis of high electronic grade semiconductors at very low temperatures to enable monolithic 3D CMOS. That has been the primary challenge in achieving such architectures. They have developed a new growth mode, where single crystalline structures of III-V's can be grown on any substrate, including amorphous oxides at ~200 °C with high carrier mobility. Current work aims at exploring to advance the use of this platform for back-end electronics and 3D CMOS. In another approach, the group is looking at semiconductors, like Te that can self-crystalize at temperatures even below room temperature arising from their unique crystal structures.

## 2.2.3 Publications (Millivolt Switches – MS)


MS1. F. Chen, H. Kam, D. Markovic, T.J. King Liu, V. Stojanovic, and E. Alon, "Integrated Circuit Design with NEM Relays," *Proc. IEEE/ACM ICCAD*, pp. 750-757, Nov 2008.

MS2. S.B. Desai, S.R. Madhvapathy, A.B. Sachid, J.P. Llinas, Q. Wang, G.H. Ahn, G. Pitner, M.J. Kim, J. Bokor, C. Hu, H.-S.P. Wong, and A. Javey, "MoS2 Transistors with 1-Nanometer Gate Lengths," *Science*, vol. 354, pp. 99-102, Oct 2016.

MS3. J.P. Llinas *et al.*, "Short-Channel Field-Effect Transistors with 9-Atom and 13-Atom Wide Graphene Nanoribbons," *Nature Communications*, vol. 8, pp. 633, Sep 2017.

MS4. Z. Mutlu, P. H. Jacobse, R. D. McCurdy, J. P. Llinas, Y. Lin, G. C. Veber, F. R. Fischer, M. F. Crommie, and J. Bokor, "Bottom-Up Synthesized Nanoporous Graphene Transistors," *Adv. Funct. Mater.*, p. 2103798, Aug 2021.

MS5. Z. Mutlu, J.P. Llinas, P.H. Jacobse, I. Piskun, R. Blackwell, M.F. Crommie, F.R. Fischer, and J. Bokor, "Transfer-Free Synthesis of Atomically Precise Graphene Nanoribbons on Insulating Substrates," *ACS Nano*, vol. 15, pp. 2635-2642, Jan 2021.

MS6. P.-C. Shen, C. Su, Y. Lin, A.-S. Chou, C.-C. Cheng, J.-H. Park, M.-H. Chiu, A.-Y. Lu, H.-L. Tang, M. M. Tavakoli, G. Pitner, X. Ji, Z. Cai, N. Mao, J. Wang, V. Tung, J. Li, J. Bokor, A. Zettl, C.-I. Wu, T. Palacios, L.-J. Li, and J. Kong, "Ultralow Contact Resistance Between Semimetal and Monolayer Semiconductors," *Nature*, vol. 593, pp. 211-217, May 2021.

MS7. C. Zhao, C. Tan, D.H. Lien, X. Song, M. Amani, M. Hettick, H.Y.Y. Nyein, Z. Yuan, L. Li, M.C. Scott, and A. Javey, "Evaporated Tellurium Thin Films for p-type Field-Effect Transistors and Circuits," *Nature Nanotechnology*, vol. 15, pp. 53-58, Jan 2020.

MS8. C. Zhao, H. Batiz, B. Yasar, H. Kim, W. Ji, M. C. Scott, D. C. Chrzan, and A. Javey, "Tellurium Single-Crystal Arrays by Low-Temperature Evaporation and Crystallization," *Adv. Mater*. vol. 33, p. 2100860, Sep 2021.

MS9. Z. A. Ye, S. Almeida, M. Rusch, A. Perlas, W. Zhang, U. Sikder, J. Jeon, V. Stojanović and T.-J. K. Liu, "Demonstration of Sub-50 mV Digital Integrated Circuits with Microelectromechnical Relays," *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec 2018.

MS10. X. Hu, S.F. Almeida, Z.A. Ye, and T.-J. King Liu, "Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications," *2019 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, pp. 34.2.1-34.2.4, Dec 2019.

MS11. U. Sikder, G. Usai, T.-T. Yen, K. Horace-Herron, L. Hutin, and T.-K. Liu, "Back-End-of-Line Nano-Electro-Mechanical Switches for Reconfigurable Interconnects," *IEEE Electron Device Letters*, vol. 41, pp. 625-628, Apr 2020.

MS12. L. P. Tatum, U. Sikder, and T.-J. K. Liu, "Design Technology Co-Optimization for Back-End-of-Line Nonvolatile NEM Switch Arrays," *IEEE Transactions on Electron Devices*, vol. 68, pp. 1471-1477, Apr 2021.

MS13. Y. -T. Wu, M. -H. Chiang, J. F. Chen, and T.-J. K. Liu, "Simulation-Based Study of High-Permittivity Inserted-Oxide FinFET with Low-Permittivity Inner Spacers," *IEEE Transactions on Electron Devices*, vol. 68, pp. 5529-5534, Nov 2021.

## 2.3 Embedded Memory

*Research activities of the Embedded Memory Thrust have been supported in part by directed membership contributions of **SK Hynix**.*

Large data sets coupled with long network latency result in significant energy inefficiencies in data centers. Processors consume energy mostly in the idle state, waiting for the network to return a data query or maintaining availability to service a remote query into local memory. Disaggregation of processing and memory resources and optimization of the network fabric, enabled by new memory technologies and silicon photonics, can provide for dramatically improved energy efficiency of warehouse-scale computers. The BETR Center research groups of **Professors Jeffrey Bokor**, **Tsu-Jae King Liu**, **Ramamoorthy Ramesh**, **Sayeef Salahuddin**, and **Vladimir Stojanović** pursue the goal of high-density non-volatile memory that can be monolithically integrated with CMOS circuitry, such as nanometer-scale magnetic and ferroelectric devices, and nano-electro-mechanical switches (NEMS) implemented in a back-end-of-line process. This research involves fundamental scientific studies, to elucidate physical phenomena such as electric-field control of magnetization in multiferroic-ferromagnet heterostructures (for voltage-controlled operation of nanomagnetic memory devices), develop ultrafast (few picoseconds) magnetic devices, as well as the integration of memory+logic fabrication processes and characterization of three-dimensionally integrated circuit structures.[EM1-EM4]

### 2.3.1 Recent Achievements

*A. Ultrafast Magnetic Switching*

The **Bokor** and **Salahuddin** groups are developing current-driven, ultra-high speed magnetic elements for logic and memory with switching energies at the sub-femtojoule level.[EM4,EM5] Magnetic systems are attractive logic switches since their non-volatility can be used to reduce static power losses. However, the low speed of magnetic switching has severely limited device applications. The BETR research team demonstrated that ultrafast

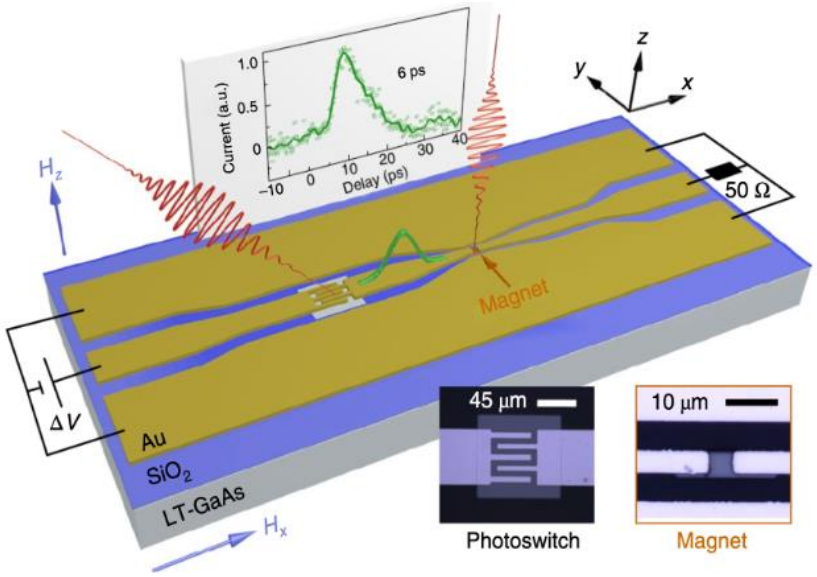



**Figure 6.** Ultrafast SOT switching set-up. Photogenerated ~6-ps-duration electrical pulses are guided and focused by a coplanar waveguide into the magnetic stack, resulting in ultrafast SOTs. The sampled picosecond current pulse is shown at the back of the figure. The solid green line is a guide to the eye.

switching of magnetic materials is possible by hot electrons that are excited via electrical pulses.[EM4] Subsequently, the group demonstrated spin-orbit torque (SOT) switching of a ferromagnet with picosecond electrical pulses.[EM5] Photoconductive switches were used to apply 6-ps-wide electrical pulses and deterministically switch the out-of-plane magnetization of a common thin cobalt film via spin–orbit torque (Figure 6).

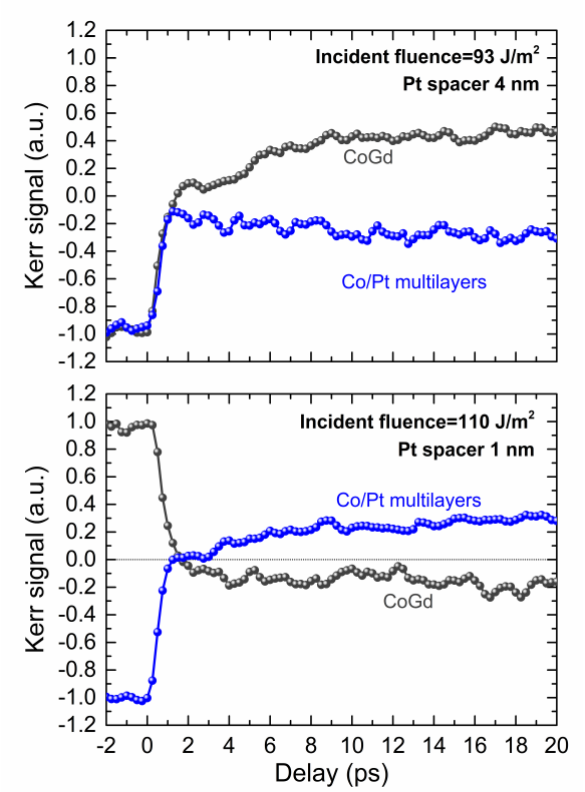



**Figure 7.** Depth-sensitive time-resolved magnetization dynamics of CoGd alloy and Co/Pt multilayers of (a) decoupled stack with 4 nm Pt spacer (top) and ferromagnetically coupled stack with 1 nm Pt spacer (bottom).

In this period, the BETR team demonstrated ultrafast exchange mediated helicity-independent all-optical switching (HI-AOS) of an exchange coupled [Co/Pt]-multilayers/Pt spacer/CoGd heterostructure.[EM6] Time-resolved magnetization dynamics were recorded selectively for the CoGd and Co/Pt layers and show switching of the Co/Pt in 3.5 ps (Figure 7), which is the fastest switching of a ferromagnet reported to date. Employing an extended microscopic three-temperature model, the temporal dynamics of the exchange coupled ferromagnet-ferrimagnet heterostructure was simulated, qualitatively and quantitatively explaining the experimental switching phenomena. This work establishes the mechanism of exchange mediated switching of ferromagnet-ferrimagnet heterostructures, which can be integrated with a magnetic tunnel junction for efficient reading after ultrafast energy-efficient switching. Furthermore, first results indicate that the magnetization switching consumes less than 50 pJ in micron-sized devices. Scaling down the device dimensions to 20 nm dimensions gives estimated switching energies of a few fJ, which is the current size of state-of-the-art magnetic memory devices.

### *B. NEM-Based Relays for Embedded Memory*

The **Liu** and **Stojanović** groups have teamed up with support by BETR industry affiliate **SK Hynix** to explore system-based integrated circuit implementations in the so-called "edge computing" scenarios, where the sensory and computation functions are severely energy limited. For example, the team has investigated the use of NEM-based relays for applications as look-up tables (LUTs) and for embedded memory, including arrays of reconfigurable NEM-based interconnects for novel memory applications.[EM3]

For this, vertically oriented relays were designed and fabricated by a standard 65nm CMOS process, using the multiple interconnect layers in the back-end-of-line (BEOL) process.[EM7,EM8] NEM switches are thus monolithically integrated with CMOS circuitry by performing a release etch after CMOS fabrication process with relatively low thermal budget. An analysis of the performance of NEMS switch-based embedded memories to increase the capacity and lower the energy-consumption per node demonstrated that with proper process node scaling, the NEMory can achieve very competitive metrics compared to CMOS-based memories and ReRAM.

In subsequent work, the team developed a multistep release-etch process for multilayered BEOL NEM switches, compatible with advanced CMOS technology nodes.[EM9] This process was used to demonstrate a hybrid CMOS-NEM circuit comprising a 4x2 BEOL non-volatile NEM switch array, fabricated using a standard 65-nm CMOS manufacturing process, for memory-based data searching (Figure 4). The array can be scaled up to accommodate large data strings on-chip. Furthermore, non-volatile and reprogrammable operation of NEM switches with air gaps as small as 32 nm, fabricated using a standard 16-nm CMOS manufacturing process, were also demonstrated, making non-volatile NEM switches a compelling candidate for future ultralow-power and datacentric computing applications.

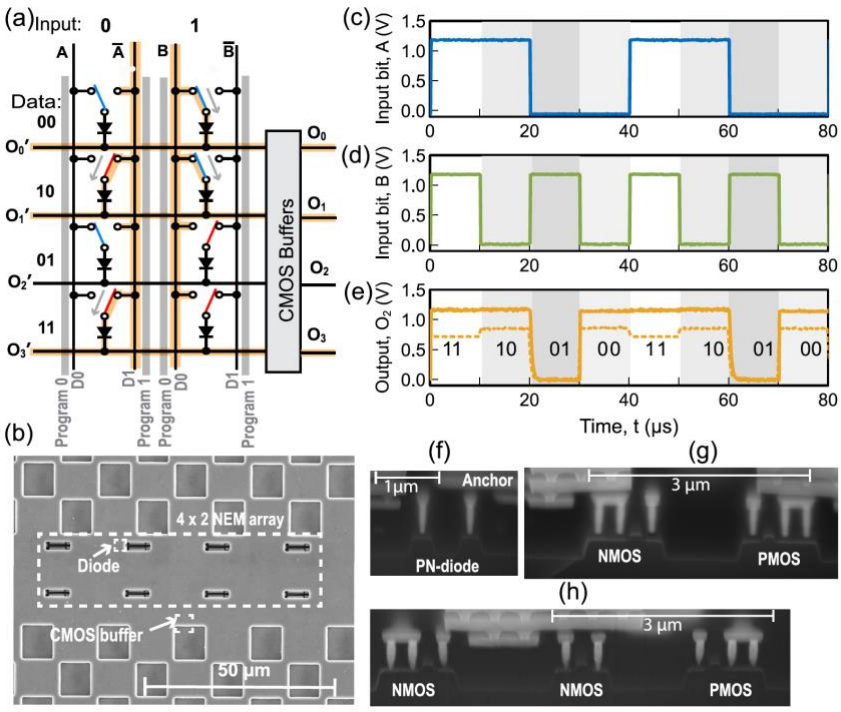



**Figure 8. a)** Circuit diagram and **(b)** plan SEM image of an NEM switch array for memory-based parallel data searching. Highlighted lines in **(a)** indicate wires that are driven to high voltage. Measured voltage waveforms for **(c)**-**(d)** input bits and **(e)** output bits demonstrate the corresponding data search operation. The dotted line in **(e)** represents the voltage on $O_2$ before passing through the CMOS buffer. SEM images showing cross-sectional view of **(f)** monolithically integrated p-n junction diode, and **(g)** first and **(h)** second stages of a monolithically integrated (gated) CMOS buffer.

### *C. Magnetoelectric Spin-Orbit (MESO) Logic*

The **Ramesh** group is exploring pathways to drastically reduce the voltage requirement for electric field switching of multiferroics. Together with colleagues from **Intel**, the team developed a new logic computing concept based on a magnetoelectric spin–orbit (MESO) device with magnetoelectric switching nodes and spin– orbit-effect readout (Figure 9).[EM10] The ultimate goal is to switch magnets purely with a voltage of just 100 mV, or below. When successful, this will

represent a 35-fold reduction in voltage amplitude compared to state of the art and a corresponding 1000-fold reduction in switching energy. This will also represent a paradigm shift in that no current will be necessary for switching magnetization.

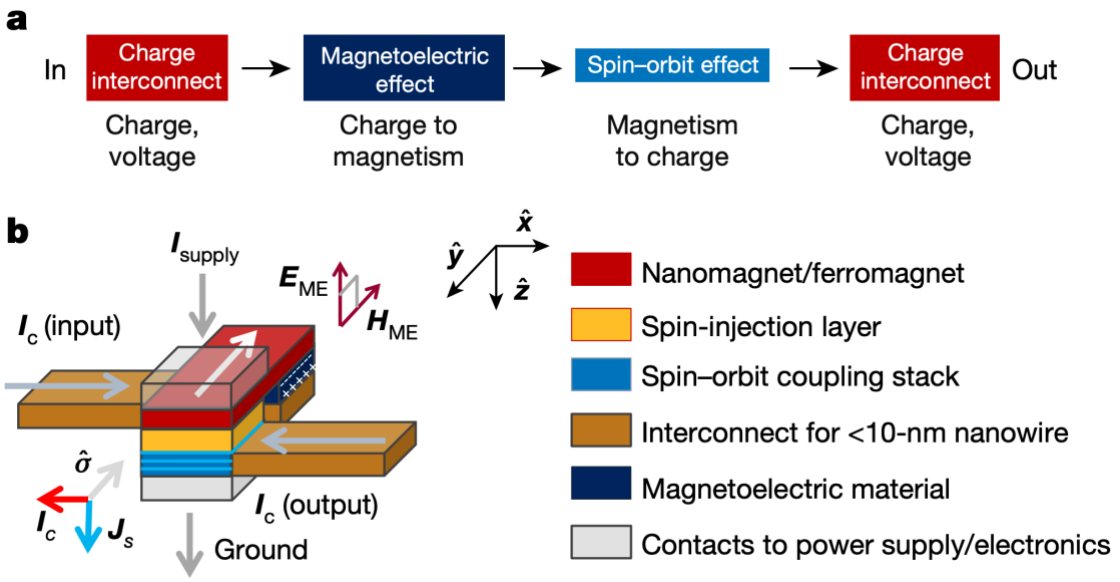



**Figure 9. a)** MESO logic transduction for a cascadable charge-input and charge-output logic device. **b)** MESO device comprising a spin-injection layer for spin injection from the ferromagnet to the topological material, an interconnect made of a conductive material, and contacts to the power supply and ground.

## 2.3.2 Current Projects

### Enabling MESO at 100 mV and Beyond

*(Prof. Ramamoorthy Ramesh)*

This project explores pathways to reduce electric field switching of multiferroics down to 100 mV using a new logic computing concept based on a magnetoelectric spin–orbit (MESO) device.[EM10] The project addresses the following challenges:

1. Is it possible to switch magnets purely with a voltage of just 100 mV? When successful, this will represent a 35X reduction in voltage amplitude compared to state of the art and a corresponding 1000X reduction in switching energy. This will also represent a paradigm shift where no current will be necessary to switch magnetization.
2. Is it possible to convert the state of a magnet into a voltage signal of the order of 100 mV? If successful, this will be 1000X improvement in the signal strength over the state of the art.
3. Is it possible to switch a magnetic order at 10s of picoseconds or less either with voltage or current? Note that this speed is ~10X faster than the state of the art and will bring spintronic devices such as memory elements at the same level as the fastest electronic memory devices with the added advantage of non-volatility and infinite endurance.

To achieve these goals, the team will pursue three approaches: (i) chemically dope $BiFeO_3$ with La and Sm to reduce its coercive voltage; (ii) reduce the thickness of $BiFeO_3$ to thicknesses as small as 10 nm, while retaining the ferroelectric/antiferromagnetic properties; (iii) explore oxide ferromagnets as the top contact.

**On-Chip Ultrafast Magnetic Switching**

*(Profs. Jeffrey Bokor, Sayeef Salahuddin, Vladimir Stojanović)*

This project builds on the recent breakthrough of ultrafast spin-orbit torque (SOT) switching of a ferromagnet with picosecond electrical pulses.[EM5] Currently, the team is exploring on-chip ultrafast magnetic switching and readout triggered by electrical pulses generated directly by CMOS circuits. Conventional CMOS scaling is projected to reach transistor speeds in the range of a few picoseconds, so such electrical pulses will be available on-chip. To take advantage of this technology, the team works on integrating magnetic device structures on advanced CMOS chips. Two challenges have to be overcome toward this goal: (1) Integration of an electrical readout into the circuit structure, and (2) reduction of both the switching energy and current to be compatible with CMOS technology. In fact, calculations revealed that energies and currents for the electrical switching of magnets could be as low as ~3.5 fJ and ~10's of μA, respectively, for a $(20\ nm)^3$ cell size.

**In-Memory and Normally-Off Computing Using Magnetic Nonvolatile Devices**

*(Profs. Jeffrey Bokor, Sayeef Salahuddin, Vladimir Stojanović)*

This project focuses on the fabrication, design, and integration of in-memory and normally-off computing using magnetic nonvolatile devices with the goal of integrating three-terminal spin-Hall memory devices with a CMOS latch. The basic idea has been to reduce power by turning off large portions of the computer that are not in use. By using non-volatile memory, the shut-down part of the computer can readily be restored to its original state, once it is needed, without needing to write to or read from external storage. By distributing the memory over the circuit (memory-in-logic), additional power savings due to reduced interconnect length can be expected. Several spin-based devices added to SRAM circuits were evaluated and analysis across a number of various benchmarks promises 35 percent energy savings with this type of memory.

## 2.3.3 Publications (Embedded Memory – EM)


EM1. E. A. Tremsina, N. Roschewsky, and S. Salahuddin, "Micromagnetic Analysis and Optimization of Spin-Orbit Torque Switching Processes in Synthetic Antiferromagnets," *Journal of Applied Physics*, vol. 126, pp. 163905, Oct 2019.

EM2. N. Roschewsky, E. Walker, P. Gowtham, S. Muschinske, F. Hellman, S. Bank, and S. Salahuddin, "Spin-Orbit Torque and Nernst Effect in Bi-Sb/Co Heterostructures," *Physical Review B*, vol. 99, pp. 195103-195108, May 2019.

EM3. K. Kato, V. Stojanović, and T.-J. K. Liu, "Embedded Nano-Electro-Mechanical Memory for Energy-Efficient Reconfigurable Logic," *IEEE Electron Device Letters*, vol. 37, pp. 1563–1565, Dec. 2016.

EM4. Y. Yang, R. Wilson, J. Gorchon, C.-H. Lambert, S. Salahuddin, and J. Bokor, "Ultrafast Magnetization Reversal by Picosecond Electrical Pulses," *Science Advances*, vol. 3, pp. E1603117, Nov 2017.
EM5. K. Jhuria, J. Hohlfeld, A. Pattabi, E. Martin, A. Y. Arriola Córdova, X. Shi, R. Lo Conte, S. Petit-Watelot, J. C. Rojas-Sanchez, G. Malinowski, S. Mangin, A. Lemaître, M. Hehn, J. Bokor, R. B. Wilson, and J. Gorchon, "Spin–Orbit Torque Switching of a Ferromagnet with Picosecond Electrical Pulses," *Nature Electronics*, vol. 3, pp. 680-686, Oct 2020.
EM6. J. Chatterjee, D. Polley, A. Pattabi, H. Jang, S. Salahuddin, and J. Bokor, "RKKY Exchange Bias Mediated Ultrafast All-Optical Switching of a Ferromagnet," *Adv. Funct. Mater.*, p. 2107490, Nov 2021.
EM7. U. Sikder, G. Usai, T.-T. Yen, K. Horace-Herron, L. Hutin, and T.-J.K. Liu, "Back-End-of-Line Nano-Electro-Mechanical Switches for Reconfigurable Interconnects," *IEEE Electron Device Letters*, vol. 41, pp. 625-628, April 2020.
EM8. U. Sikder, L.P. Tatum, T.-T. Yen, and T.-J.K. Liu, "Vertical NEM Switches in CMOS Back-End-of-Line: First Experimental Demonstration and Programming Scheme," *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, pp. 21.2.1-4, Mar 2021.
EM9. U. Sikder, K. Horace-Herron, T.-T. Yen, G. Usai, L. Hutin, V. Stojanović, and T.-J. King Liu, "Toward Monolithically Integrated Hybrid CMOS-NEM Circuits," *IEEE Transactions on Electron Devices*, vol. 68, pp. 6430-6436, Dec 2021.
EM10. S. Manipatruni, D.E. Nikonov, C.-C. Lin, T.A. Gosavi, H. Liu, B. Prasad, Y.-L. Huang, E. Bonturim, R. Ramesh, and I.A. Young, "Scalable Energy-Efficient Magnetoelectric Spin-Orbit Logic," *Nature*, vol. 565, pp. 35-43, Jan 2019.

## 2.4 Flexible and Wearable Electronics

The goal of the Wearable and Flexible Electronics research areas in the BETR Center is to develop a new manufacturing and deployment paradigm for wearable, interactive information devices, including displays, sensors, and logic devices. Research activities are guided by the recognition that electronic devices must be non-intrusive, easily deployed and inexpensive, to become a pervasive technology. Spearheaded by the research groups of **Prof. Ali Javey** and **Prof. Ana Arias**, wearable and flexible electronics research in the BETR Center entails the development of tools, processes and materials for roll-to-roll processing, layer transfer, high-resolution printing, thin-film development, and packaging.[FE1,FE2] An overview on recent developments in wearable biosensing is presented in a review by the **Javey** group in *Advanced Functional Materials*.[FE3]

### 2.4.1 Recent Achievements

*A. Wearable Electronics for Sweat Monitoring*

The **Javey** group used its expertise in microfluidics to design and fabricate wearable electronic patches for continuous sweat monitoring at rest.[FE4] The microfluidic design was optimized to combat evaporation, enable selective monitoring of secretion rate, and reduce required sweat accumulation times. In fact, the group developed a wearable device for rapid uptake of nL $min^{-1}$ $cm^{-2}$ rates of thermoregulatory sweat at rest, enabling near-real-time sweat rate and composition analysis at rest (Figure 10). Along with sweat rate sensors, the team also integrated electrochemical sensors for pH, chloride ion, and levodopa monitoring. They demonstrate patch functionality for dynamic sweat analysis related to routine activities, stress events, hypoglycemia-induced sweating, and Parkinson's disease, thus enabling continuous, autonomous monitoring of body physiology at rest. More generally, the developed patch can be used to study correlations between sweat rates and composition, helping to better understand analyte secretion mechanisms and guide how measured concentrations should be interpreted. Recently, the group also presented wearable sweat sensors with convenient glove-based form factors for sweat sensing under routine and even sedentary activity, making sweat-based biomarker monitoring practical for daily life.[FE5]

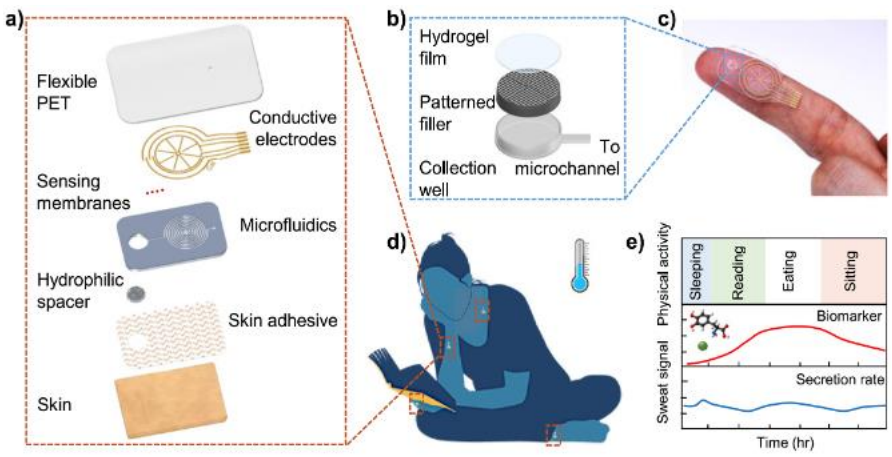



**Figure 10.** Schematic of the microfluidic sweat analysis patch containing multiple layers (a) and a hydrophilic filler to enhance sweat collection (b). An optical image of the sweat patch on a user's finger (c), or worn on various body locations (d), while continuously monitor both sweat secretion rate and compositions for long-term without external sweat stimulation (e).

### *B. Stencil-Printing of Li-ion Miniature Batteries*

The **Arias** group is developing various device fabrication methods based on roll-to-roll printing (screen and inkjet printing), blade coating, and organic binding techniques. For example, the team developed printed flexible composite Zn/$MnO_2$ batteries using organic gels as binder for the $MnO_2$ electrode.[FE6] Recently, the group also introduced fully flexible ambient light pulse oximeters from new organic photodiodes compatible with roll-to-roll printing techniques.[FE7] These new wearable devices can be combined with wireless data transmission capability. They demonstrated that these flexible devices accurately detect varying oxygen saturation levels in the body.

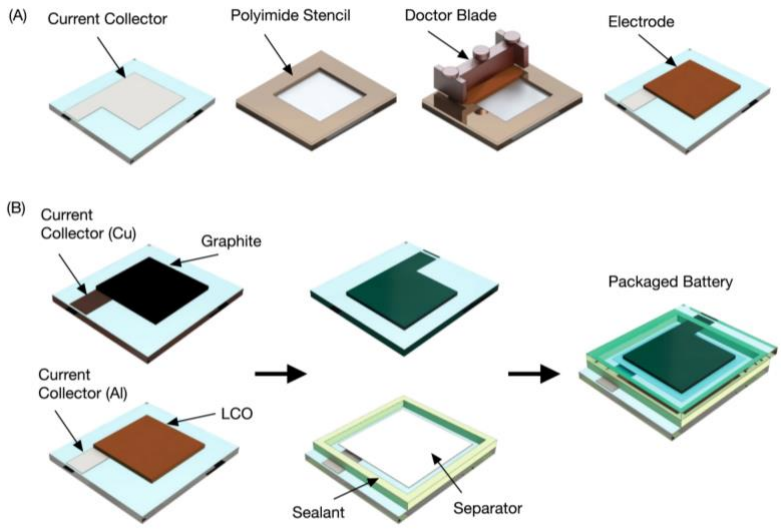



**Figure 11. A)** Stencil printing process: A plastic stencil with the square electrode pattern is placed on the substrate, and a doctor blade is moved over the stencil, which pushes the ink into the stencil, forming the printed film. **B)** Schematic representation of the battery fabrication process. First, the anode (graphite) and cathode (LCO) slurries were deposited over the Cu and Al current collectors, respectively, using stencil printing. The miniature Li-ion batteries were prepared by stacking the cathode and anode with a polypropylene separator (soaked in LiPF6 electrolyte) and packaging using an adhesive sealant.

In this period, the **Arias** group developed a battery design and fabrication process for miniature lithium-ion (Li-ion) batteries, which are ideal candidates for powering IoT devices.[FE8] These new Li-ion mini-batteries, with active areas as small as 1 $mm^2$, displayed high areal capacities and energy densities and were fabricated by combining a stencil printing process to deposit thick high-capacity electrodes with an adhesive based battery sealing method (Figure 11). The fabricated mini-batteries demonstrated a significantly higher discharge capacity (6.4 $mAh/cm^2$) and energy density (23.6 $mWh/cm^2$) than thin-film and thick-film, and 3D micro-batteries. The team demonstrated that the capacity of the battery is sufficient to support the power requirements of a MEMS-based wireless sensor system with peak current requirements as high as 4 mA. The new batteries are excellent candidates for integrated electronics requiring a power source with high energy density and small footprint, such as in autonomous wireless sensor nodes, and miniaturized electronic systems in medical devices.

### *C. Electronic Skin by Mechanotransduction*

Inspired by the skin's sensory behavior, the **Arias** group previously introduced a potentiometric mechanotransduction mechanism, which allows to encode mechanical stimuli into potential differences measured between two electrodes.[FE9] The devices were fabricated by an all-solution processing technique and exhibited ultralow-power consumption, high tunability, and a good

capability to detect both static and low-frequency dynamic mechanical stimuli. Based on this sensing mechanism, the group introduced two novel devices: (i) stretchable mechanical sensors with strain-independent performance and (ii) single-electrode-mode e-skins with better pixel density and data acquisition speed compared with traditional dual-electrode-mode e-skins.

Recently, the **Arias** group expanded this concept by demonstrating a potentiometric e-skin for simultaneous thermosensation and mechanosensation, based on thermally regulated intrinsic impedance variation of the electrolyte and mechanically regulated electrode/electrolyte interfacial impedance variation, respectively (Figure 12).[FE10] This approach allows monitoring of both static and dynamic thermal or mechanical stimuli without an external power supply, compensating for the deficiencies of existing passive sensing devices. Leveraging this potentiometric sensing scheme, the group also demonstrated a soft robotic gripper and a passive e-skin for both thermosensation and mechanosensation. The new e-skin features a single-electrode configuration, all-solution-processing fabrication, simplified operation, ultralow power consumption, ultrahigh sensitivity, and good capability for simultaneous temperature mapping and pressure mapping. This potentiometric e-skin can find promising applications in the emerging fields of skin prosthetics, humanoid robotics, wearable healthcare devices, bioelectronics, and other smart systems.

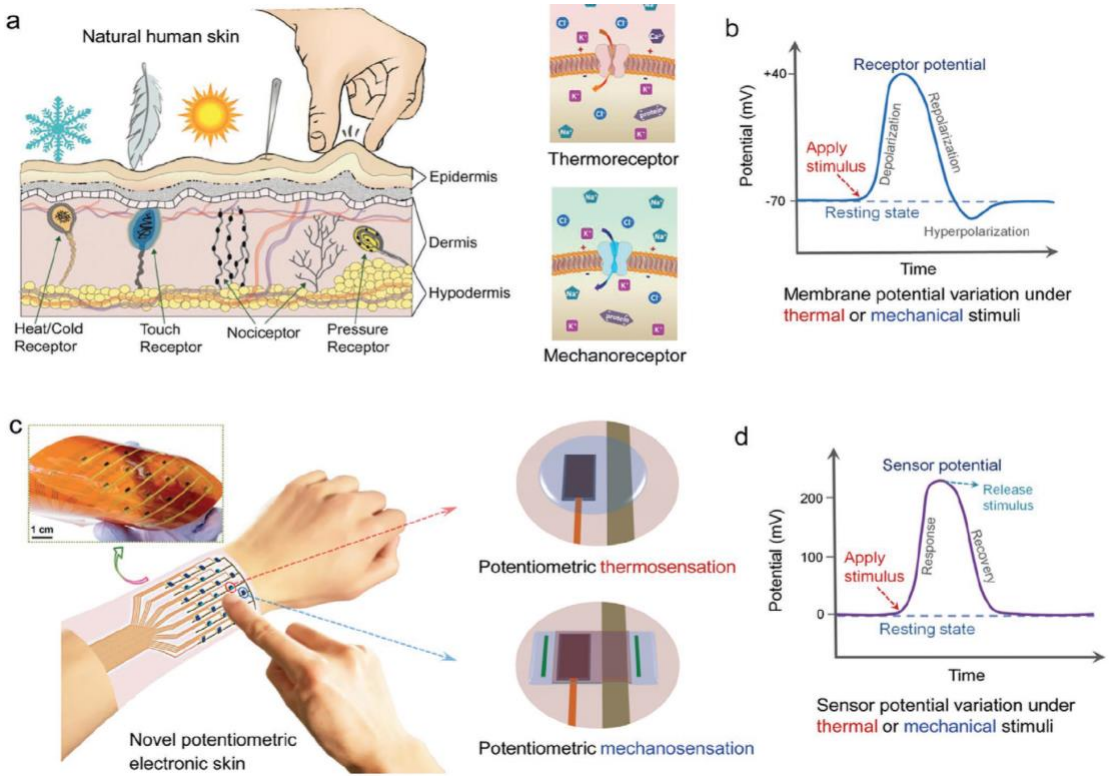



**Figure 12.** Bioinspired design of potentiometric e-skin for both thermosensation and mechanosensation. **a)** Illustrations depicting the thermoreceptors and mechanoreceptors in natural skin sensory system. **b)** Schematic showing the response behaviors of natural thermoreceptors and mechanoreceptors to external stimuli based on the variation in membrane potential. **c)** Photograph and schematics showing an artificial e-skin based on a single potentiometric sensing scheme for both thermosensation and mechanosensation. **d)** Schematic illustrating the response behaviors of the potentiometric thermal sensors and mechanical sensors to external stimuli based on the variation in sensor potential.

## 2.4.2 Current Projects

**Wearable Sensors for Non-Invasive Continuous Monitoring of Biomarkers**
*(Prof. Ali Javey)*

The goal of this proposal is to develop non-invasive sensors that can continuously monitor the concentrations of clinically relevant biomarkers in readily accessible bodily fluids, such as sweat.[FE1,FE3,FE4] The sensors will be used to perform medium to large scale population studies with vast time-series of data to generate personalized baselines indicative of the user's health. Over the last several years, the Javey group has developed a portfolio of wearable electrochemical sensors generally consisting of two main components that are interfaced together: (i) disposable sensor patch, and (ii) reusable electronics for signal condition, processing and transmission. They have developed roll-to-roll fabrication schemes for the sensor patches to enable a cost-effective method of mass producing the sensors through our collaboration with external partners, including VTT. The group has demonstrated small scale population studies to observe preliminary correlations for certain analytes, including pH, $Cl^-$, $Na^+$, vitamin C, nicotine, caffeine, and levodopa.

## 2.4.3 Publications (Flexible Electronics – FE)


FE1. Y. Yu, H.Y.Y. Nyein, W. Gao, and A. Javey, "Flexible Electrochemical Bioelectronics: The Rise of In Situ Bioanalysis," *Advanced Materials*, vol. 32, pp. 1902083, Apr 2020.

FE2. Y. Khan, A. Thielens, S. Muin, J. Ting, C. Baumbauer, and A.C. Arias, "A New Frontier of Printed Electronics: Flexible Hybrid Electronics," *Advanced Materials*, vol. 32, pp. 1905279, Apr 2020.

FE3. Y. Lin, M. Bariya, and A. Javey, "Wearable Biosensors for Body Computing," *Adv. Funct. Mater.*, vol. 31, p. 2008087, Sep 2021.

FE4. H.Y.Y. Nyein, M. Bariya, B. Tran, C.H. Ahn, B.J. Brown, W. Ji, N. Davis, and A. Javey, "A Wearable Patch for Continuous Analysis of Thermoregulatory Sweat at Rest," *Nature Communications*, vol. 12, pp. 1823, Mar 2021.

FE5. M. Bariya, L. Li, R. Ghattamaneni, C.H. Ahn, H.Y.Y. Nyein, L.-C. Tai, and A. Javey, "Glove-Based Sensors for Multimodal Monitoring of Natural Sweat," *Science Advances*, vol. 6, pp. eabb8308, Aug 2020.

FE6. A.M. Zamarayeva, A. Jegraj, A. Toor, V.I. Pister, C. Chang, A. Chou, J.W. Evans, and A.C. Arias, "Electrode Composite for Flexible Zinc–Manganese Dioxide Batteries through In Situ Polymerization of Polymer Hydrogel," *Energy Technology*, vol. 8, pp. 1901165, Mar 2020.

FE7. D. Han, Y. Khan, J. Ting, J. Zhu, C. Combe, A. Wadsworth, I. McCulloch, and A.C. Arias, "Pulse Oximetry Using Organic Optoelectronics under Ambient Light," *Advanced Materials Technologies*, vol. 5, pp. 1901122, May 2020.

FE8. A. Toor, A. Wen, F. Maksimovic, A. M. Gaikwad, K. S. J. Pister, and A. C. Arias, "Stencil-printed Lithium-ion micro batteries for IoT applications," Nano Energy, vol. 82, p. 105666, Apr 2021.

FE9. X. Wu, M. Ahmed, Y. Khan, M.E. Payne, J. Zhu, C. Lu, J.W. Evans, and A.C. Arias, "A Potentiometric Mechanotransduction Mechanism for Novel Electronic Skins," *Science Advances*, vol. 6, pp. eaba1062, Jul 2020.

FE10. X. Wu, J. Zhu, J. W. Evans, C. Lu, and A. C. Arias, "A Potentiometric Electronic Skin for Thermosensation and Mechanosensation," *Advanced Functional Materials*, vol. 31, p. 2010824, Apr 2021.

## 2.5 Hardware Accelerators for AI

The emergence of machine learning and other artificial intelligence applications has been accompanied by a growing need for new hardware architectures. The BETR Center research groups of **Professors Tsu-Jae King Liu**, **Sayeef Salahuddin**, **Sophia Shao, Vladimir Stojanović**, **Laura Waller**, and **Eli Yablonovitch** are investigating hardware accelerators specialized for large-scale matrix computations used in deep neural networks.[AI1-AI4] The BETR Center also develops new machines for solving difficult combinatorial optimization problems, such as those found in operations research, finance, and circuit design. The conventional von-Neumann computer is ill-suited for these applications in terms of latency and energy efficiency, due to its intrinsic architectural and algorithmic limitations, opening the door for alternative physical systems based on emerging technologies. BETR Center researchers investigate deep neural networks based on novel logic switches, architecture-aware network pruning techniques, systematic optimization strategies of deep learning architectures, and analog machines that can solve NP-hard optimization problems without the need for the complexity of quantum bits.

### 2.5.1 Recent Achievements

*A. Optimized Scheduling of Deep Neural Networks*

State-of-the-art deep neural networks (DNNs) employ specialized DNN accelerators, many of which feature a large number of processing elements laid out spatially, together with a multi-level memory hierarchy and flexible interconnect. Management of how computation is scheduled both spatially and temporally has thus become increasingly important for optimized computation. In fact, different scheduling choices can lead to wide variations in performance and efficiency, motivating the need for a fast and efficient search strategy to navigate the vast scheduling space.

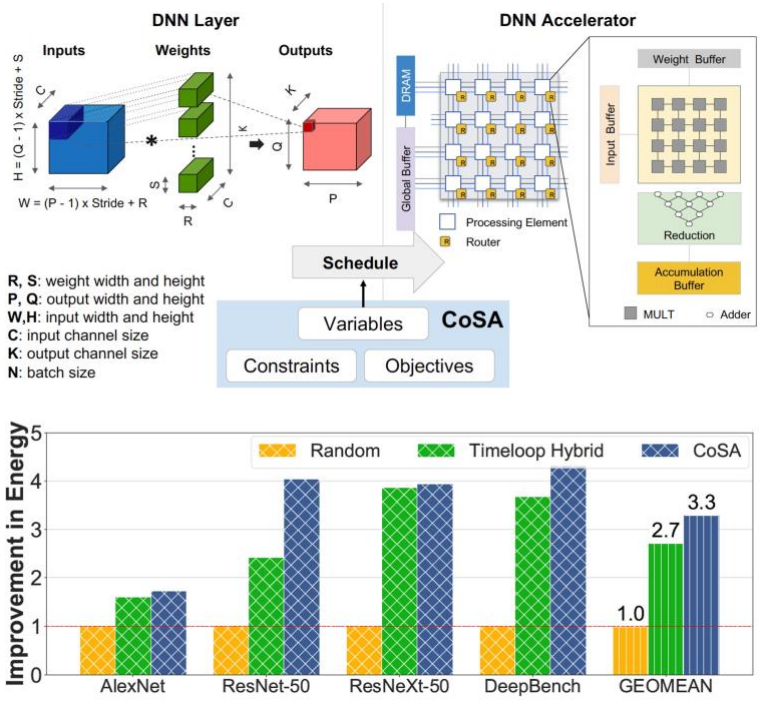



**Figure 13. Top.** DNN scheduling problem formulation with CoSA. CoSA takes 1) DNN layer dimensions and 2) DNN accelerator parameters and expresses the scheduling problem into a constrained optimization problem to produce a performant schedule in one shot. **Bottom.** Improvements in total network energy reported by the Timeloop energy model.

The **Shao** group has addressed this very challenge and developed CoSA, which is a

constrained optimization-based approach for scheduling DNN accelerators.[AI5] As opposed to existing approaches that either rely on designers' heuristics or iterative methods to navigate the search space, CoSA expresses scheduling decisions as a constrained-optimization problem that can be deterministically solved using mathematical optimization techniques. Specifically, CoSA leverages the regularities in DNN operators and hardware to formulate the DNN scheduling space into a mixed-integer programming (MIP) problem with algorithmic and architectural constraints, which can be solved to automatically generate a highly efficient schedule in one shot (Figure 13, top). The group demonstrated that CoSA-generated schedules greatly improve total network energy requirements (Figure 13, bottom) and significantly outperform state-of-the-art approaches by a geometric mean of up to 2.5 times across a wide range of DNN networks while improving the time-to-solution by a factor of 90.

### *B. Domain-Specific Accelerator Design*

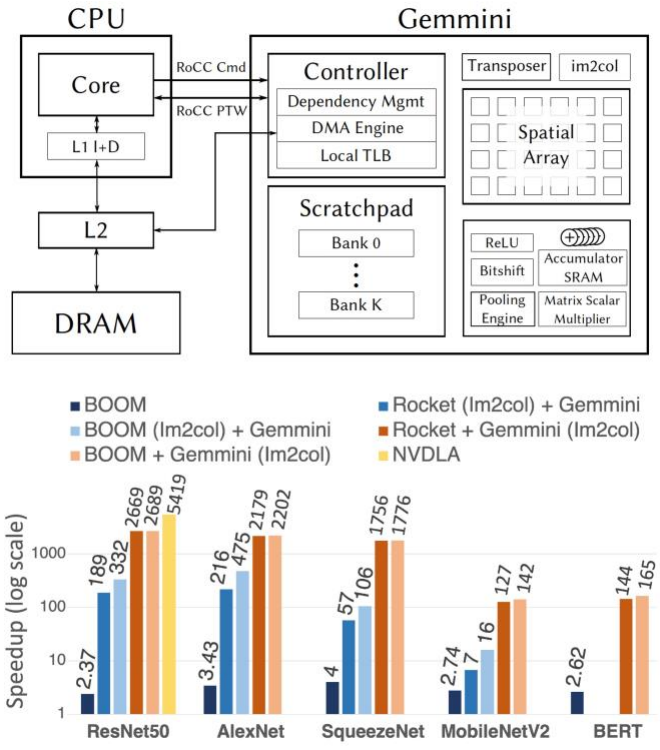



**Figure 14. Top:** Gemmini hardware architectural template overview. **Bottom:** Gemmini-produced speedup compared to an in-order CPU baseline. For CNNs, im2col was performed on either the CPU, or on the accelerator.

The **Shao** group has developed a full-stack, open-source generator of DNN accelerators that enables systematic evaluations of DNN accelerator architectures.[AI6] This new generator, named Gemmini, leverages a flexible architectural template to capture different flavors of DNN accelerator architectures, and therefore, directly addresses current issues with DNN accelerators, which are often developed and evaluated in isolation without considering the cross-stack, system-level effects in real-world environments (Figure 14, top). This makes it difficult to appreciate the impact of System-on-Chip (SoC) resource contention, OS overheads, and programming stack inefficiencies on overall performance and energy-efficiency. Gemmini generates a wide design-space of efficient ASIC accelerators from a flexible architectural template, together with flexible programming stacks and full SoCs with shared resources that capture system-level effects. The team has also fabricated Gemmini-generated accelerators and showed that they deliver up to three orders-of-magnitude speedups over high-performance CPUs on various DNN benchmarks (Figure 14, bottom). These case studies show how accelerator designers and system architects can use Gemmini to co-design and evaluate system-level behavior in emerging applications. Gemmini is open-sourced at https://github.com/ucb-bar/gemmini.

### *C. Restricted Boltzmann Machine Neural Networks*

The **Salahuddin** group successfully used the Restricted Boltzmann Machine (RBM) as a stochastic neural network capable of solving NP-Hard combinatorial optimization problems efficiently.[AI7] By exploiting the intrinsic parallelism present in the RBM architecture on a flexible Field Programmable Gate Array (FPGA) based accelerator, the team showed that this sampling framework is competitive with state-of-the-art computing machines based on novel physics. In agreement with the findings by the **Yablonovitch** group,[AI2] this work showed that it is possible to substantially accelerate computationally difficult problems using classical hardware.

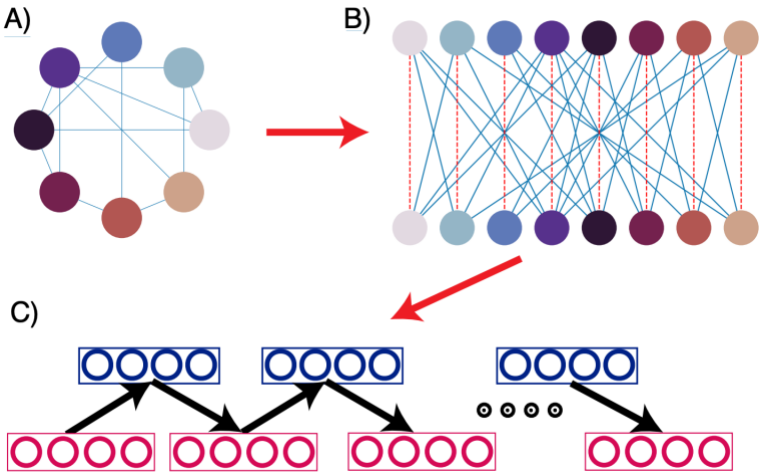



**Figure 15.** Demonstration of RBM structure and sampling algorithm. **A)** Structure of the input graph for an Ising model type algorithm. The graph is fully connected, with no restrictions on the size or magnitude of the weight matrix. **B)** Mapping of the Ising model to an RBM. **C)** Parallel sampling layers.

The RBM structure and sampling algorithm were demonstrated for an Ising model problem (Figure 15). The input graph for the Ising model type algorithm is fully connected, with no restrictions on the size or magnitude of the weight matrix (Figure 15A). The Ising model is then mapped to an RBM by making two copies of each graph node and edge and arranging them into a bipartite graph (Figure 15B). One copy is in the "visible" layer neurons and one in the "hidden" layer neurons, with no intra-layer edges. Each physical copy of the neuron is connected by a "coupling" parameter, *C*, which constrains the two copies to be the same value. Due to the lack of intra-layer connections, the layers can be sampled in parallel (Figure 15C). Each of the neurons in a layer is sampled in parallel and used to calculate the values of the opposite layer, creating a two-step sampling procedure. This sampling procedure proceeds until the output of the algorithm has reached the ground state, or until the algorithm output is of sufficient quality. The **Salahuddin** group benchmarked the RBM against the DWave 2000Q Quantum Adiabatic Computer and the Optical Coherent Ising Machine on two such optimization problems: the MAX-CUT problem and finding the ground state of a Sherrington-Kirkpatrick (SK) spin glass. On these problems, the hardware accelerated RBM shows best in class performance compared to these other accelerators, with an empirical scaling performance for probability of reaching the ground state. The results revealed up to $10^7$-fold and $10^5$-fold time to solution improvement compared to the DWave 2000Q on the MAX-CUT and SK problems, respectively, along with a 200-fold and 1000-fold performance increase compared to the Coherent Ising Machine annealer. By using commodity hardware running at room temperature for acceleration, the RBM also has greater potential for immediate and scalable use.

### 2.5.2 Current Projects

**Photonic and Analog-Mixed Signal Generators**

*(Prof. Vladimir Stojanović)*

The Stojanović group is developing design automation tools for photonic and AMS design. Berkeley Photonic Generator has been developed to streamline the design and optimization of complex layout shapes needed for silicon-photonic designs for various applications. It plugs directly into the Berkeley Analog Generator framework enabling photonic-ams co-design. The BPG framework is open-source and contains generator libraries for a large array of silicon-photonic components. The generator is structured in a way to support compilation of the photonic components into different foundry process kits, from the same generator base. They are also developing AI/ML based design automation methods on top of BAG to enable AMS circuits process porting and topology optimization.

**Physics-Based Digital Optimization**

*(Prof. Eli Yablonovitch)*

Optimization is vital to engineering, artificial intelligence, control theory and many areas of science. Mathematically, we usually employ steepest-descent, or other digital algorithms, however, physics itself, performs optimizations in the normal course of dynamical evolution. Nature provides us with the following optimization principles: (1) The Principle of Least Action; (2) The Variational Principle of Quantum Mechanics; (3) The Principle of Minimum Entropy Generation; (4) The First Mode to Threshold Method; (5) The Principle of Least Time; (6) The Adiabatic Evolution Method; (7) Quantum Annealing. In effect, physics can provide machines which solve digital optimization problems much faster than any digital computer. Of these physics-based principles, "Minimum Entropy Generation" in the form of bistable electrical or optical circuits is particularly adaptable toward offering digital optimization.

**Domain-Specific Accelerator Design**

*(Prof. Sophia Shao)*

The Shao group is developing modular, high-performance, and reusable domain-specific accelerators for emerging applications like deep learning, robotics, and graphics.[AI6] They aim to build an efficient and reusable infrastructure to enable designers to significantly improve the design productivity. The group is also interested in building machine-learning-driven design space exploration tools to quickly explore the large design space of accelerators.

**Accelerator Integration**

*(Prof. Sophia Shao)*

The Shao group is developing systematic methodologies and optimizations to enable efficient accelerator integration with the rest of System-on-Chip and/or System-in-Package. The goal is to holistically understand the system-level interactions across accelerators, general-purpose cores, and shared resources so that they can efficiently execute a wide range of applications in future-generation of SoCs and SiPs.

**Accelerator Programming Infrastructure**

*(Prof. Sophia Shao)*

The Shao group is building high-productivity programming infrastructure to enable fast and efficient mapping of applications to domain-specific systems. In particular, they leverage the regularity in both applications and domain-specific systems and formulate the programming problems as a constrained-optimization problem.[AI5] The group demonstrated that by leveraging advances in integer-linear programming and deep reinforcement learning, they can quickly find performant scheduling solutions without going through expensive, brute-force search.

**Stochastic Neural Networks Based on Restricted Boltzmann Machines**

*(Prof. Sayeef Salahuddin)*

The Salahudding group recently demonstrated that a restricted Boltzmann machine (RBM) can solve NP-Hard combinatorial optimization problems by exploiting the intrinsic parallelism present in the RBM architecture on a flexible Field Programmable Gate Array (FPGA) based accelerator.[AI7] The goal of this project is to show that further accelerator-level parallelization and scaling are possible through the use of multi-FPGA designs and communication, time division multiplexing, and more efficient pipeline stages. This will open the possibility of using parallel, stochastic computing to solve NP-Hard and NP-Complete problems with far reaching consequences in fields like logistics, scheduling, resource allocation, and many others.

## 2.5.3 Publications (Artificial Intelligence – AI)


AI1. L. Supic, R. Naous, R. Sredojevic, A. Faust, and V. Stojanović, "MPDCompress - Matrix Permutation Decomposition Algorithm for Deep Neural Network Compression," *arXiv*:1805.12085, May 2018.

AI2. S. K. Vadlamani, T. P. Xiao, and E. Yablonovitch, "Physics Successfully Implements Lagrange Multiplier Optimization," *Proceedings of the National Academy of Sciences*, vol. 117, no. 43, pp. 26639-26650, Oct 2020.

AI3. M. Kellman, M. Lustig, L. Waller, "How to do Physics-based Learning," *arXiv*:2005.13531, May 2020.

AI4. K. Hakhamaneshi, N. Werblun, P. Abbeel, and V. Stojanovic, "BagNet: Berkeley Analog Generator with Layout Optimizer Boosted with Deep Neural Networks," *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA, 2019, pp. 1-8, Jan 2020.

AI5. Q. Huang, A. Kalaiah, M. Kang, J. Demmel, G. Dinh, J. Wawrzynek, T. Norell, and Y. S. Shao, "CoSA: Scheduling by Constrained Optimization for Spatial Accelerators," *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA)*, pp. 554-566, Aug 2021.

AI6. H. Genc, S. Kim, A. Amid, A. Haj-Ali, V. Iyer, P. Prakash, J. Zhao, D. Grubb, H. Liew, H. Mao, A. Ou, C. Schmidt, S. Steffl, J. Wright, I. Stoica, J. Ragan-Kelley, K. Asanovic, B. Nikolic, and Y. S. Shao, "Gemmini: Enabling Systematic Deep-Learning Architecture Evaluation via Full-Stack Integration," *Design Automation Conference (DAC)*, PREPRINT, Dec 2021.

AI7. S. Patel, P. Canoza, and S. Salahuddin, "Logically Synthesized and Hardware-Accelerated Restricted Boltzmann Machines for Combinatorial Optimization and Integer Factorization," *Nature Electronics*, vol. 5, pp. 92-101, Feb 2022.

## 2.6 System Integration

Future information and communication (ICT) applications set a broad context for research conducted in the BETR Center research groups of **Professors Jeffrey Bokor**, **Tsu-Jae King Liu**, **Sophia Shao**, and **Vladimir Stojanović**. While system integration research efforts in the BETR Center are complementary to other industry-sponsored centers such as the Berkeley Wireless Research Center (BWRC), collaborative projects with BWRC serve to bridge innovations in physical electronics together with innovations in IC design, for co-optimization of new solid-state device technologies and computer architectures.[SI1-SI4] Through device modeling and simulation of integrated systems, tradeoffs between energy efficiency and performance can be optimized for a wide range of applications.

### 2.6.1 Recent Achievements

*A. Ultrafast Electronic-Photonic Egress Link*

While quantum computing and superconducting logic-based high-performance computing are gaining ground, the interconnection technology between cryogenic and room temperature environments has become one of the bottlenecks. Electronic-photonic (E/O) links due to the negligible heat transfer and high communication throughput are promising candidates, however, most systems require additional cryogenic amplifier stages to connect with superconducting electronics, rendering them energy-inefficient in terms of the overall system power dissipation.

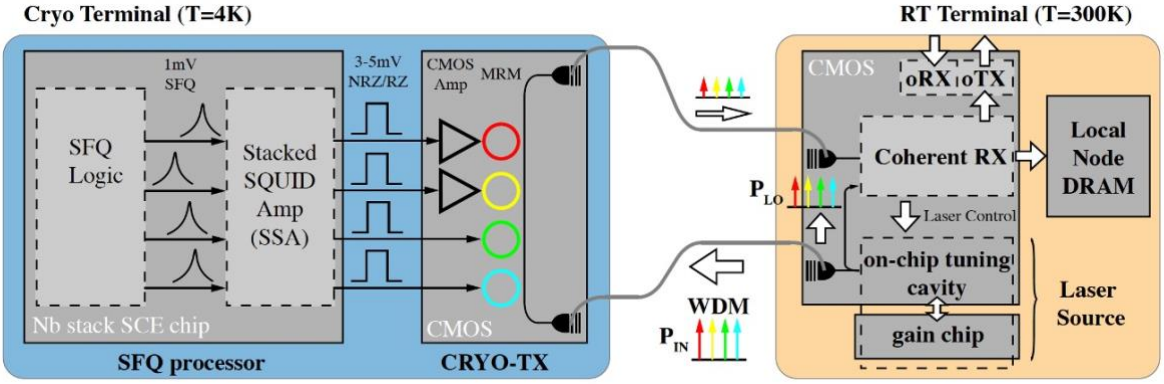



**Figure 16.** Proposed electronic-photonic egress link connecting cryo compute node with room temperature (RT) main memory.

To address this issue, the **Stojanović** group proposed a novel Coherent Ultrafast Reflective Link (CURL) as the solution for the cryogenic data egress link by leveraging the large energy cost asymmetry between cryogenic and room temperature environments (Figure 16).[SI5] The whole system, rather than a single device, is analyzed to find the optimum link energy efficiency. As the first prototype of this link, an electro-optical transmitter with CMOS pre-amplifier and ring-resonator based optical modulator was fabricated in a 45RFSOI CMOS process and characterized at the cryogenic temperature within the CURL link setup. Measurement results show that this

optical transmitter can be directly driven by superconducting electronics with millivolt-level voltage swing, and the new link has five times better energy efficiency than the traditional intensity modulation, direct-detection (IMDD) link.

### *B. Relay-Based Digital Integrated Circuits*

The **Liu**, in collaboration with the **Stojanović** group, has demonstrated reliable operation of relay-based digital integrated circuits (ICs) with 50 mV supply voltage.[SI2,SI3] No other digital IC device technology developed to date has even been projected to be able to operate at such low voltages at room temperature. Recently, the team developed a method to fabricate back-end-of-line (BEOL) non-volatile NEM switches (NV-NEM) switches with minimum (100-nm) contact/actuation gaps, which incorporates a post-foundry release-etch process that is fully compatible with the BEOL material stack.[SI6] The new process enables leveraging multiple CMOS BEOL layers for NEM switches, which is advantageous for achieving lower programming voltage and/or more compact footprint. A functional array of BEOL NV-NEM switches is used to implement a hybrid CMOS-NEM IC for data search applications.

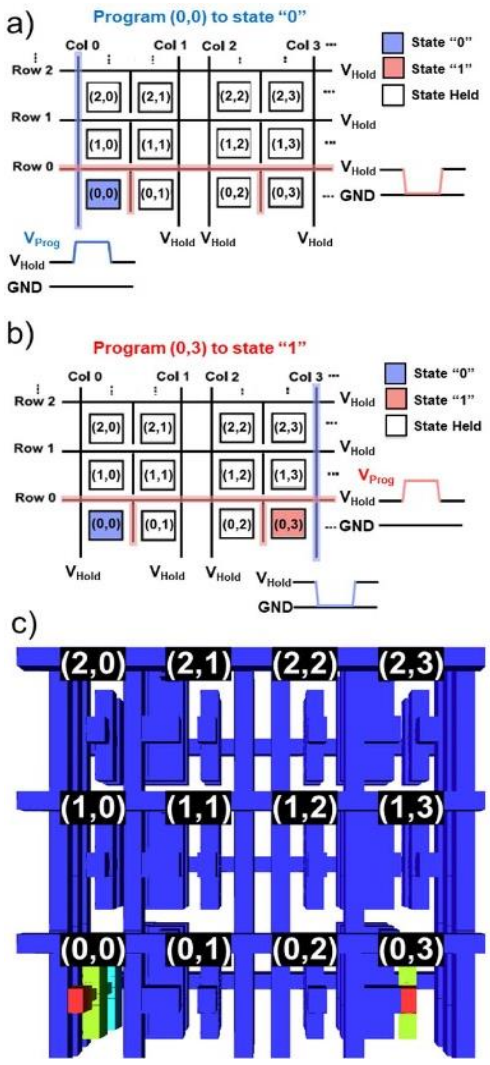



**Figure 17.** Circuit schematics of a 3x4 array of NV-NEM bit-cells, showing the voltage pulses applied to the row and column address lines to program bit-cell **(a)** (0.0) to state "0" and **(b)** (0.3) to state "1." **(c)** Layout view of the corresponding 3x4 array of NV-NEM bit-cells.

In this period, the **Liu** group also presented a crossbar array architecture of vertically oriented BEOL NV-NEM switches.[SI7] The team demonstrated that optimally designed NV-NEM switches implemented with three BEOL layers in a 5-nm CMOS technology can be programmed with CMOS-compatible voltages and are expected to be more compact than SRAM cells. Simulation results indicated that sub-20-ns programming delay is possible with programming voltages compatible with standard input-output (I/O) CMOS circuitry, and that the write energy of an NV-NEM bit-cell will be less than 5 aJ—much more energy-efficient than any other type of NVM device. A crossbar array architecture provides for high bit-cell density, and a half-select programming scheme effectively eliminates the need for access transistors without causing write disturb issues (Figure 17). The scaled NV-NEM switch technology shows excellent promise for embedded memory applications and will guide future design optimization of compact nanoelectromechanical relay-based switch arrays.

*C. Electronic-Photonic Lab-on-Chip Platform*

Recent worldwide challenges to healthcare systems have emphasized the need for accurate and on-demand Point-of-Care (PoC) platforms, which can provide – personalized to each patient – diagnostic and prognostic multiparametric information on various infections. In response, the **Stojanović** group is developing solutions based on electronic-photonic LoC system for biosensing.[SI8-SI10] Recently, the group presented a fully integrated arrayed monolithic electronic-photonic system-on-chip (EPSoC) platform in a zero-change high volume CMOS-SOI process, which addresses the requirements of next-generation PoC systems (Figure 18).[SI11] On-chip readout processing and control electronics eliminate the need for external readout equipment and bulky tunable lasers, drastically miniaturizing the system. Additionally, by leveraging co-integration of planar 10μm diameter micro-ring resonators (MRRs) with on-chip electronics, multi-MRR electronic-photonic arrays were enabled, unlocking key sensing capabilities in molecular sensing and ultrasound imaging. Furthermore, the team presented preliminary real-time kinetic and ultrasound imaging results using two first generation EPSoCs fabricated in a high volume commercial GF45nm process, demonstrating that complete and self-contained Lab-on-Chip (LoC) systems capable of providing multiparametric biosensing information are possible.

## 2.6.2 Current Projects

**SuperFabric**

*(Prof. Vladimir Stojanović)*

SuperFabric looks at design of WDM photonic links that work together with a MEMS-based optical switch (high-radix 128-1024 with sub-us switching time) to aid in scale-out of compute clusters for AI training. The photonic links have fast (sub-100ns) electro-optic wavelength lock and burst-mode CDR and laser forwarding to mitigate switch insertion losses.

**mm-Wave Photonic WDM Links for Radar Phase-Array and Massive-MIMO Systems**

*(Prof. Vladimir Stojanović)*

The goal of this project is to design antenna-to-photons analog mm-wave photonic links that minimize the power consumption at the phase-array panel, by converting mm-wave signals from the antenna directly to the optical domain with a mm-wave LNA chain directly modulating ring modulators specialized for mm-wave modulation. The remoted central processing site receivers use coherent demodulation to avoid mm-wave mixers and simplify the mm-wave receiver front-ends.

**Relay-Based Digital Integrated Circuits**

*(Prof. Tsu-Jae King Liu)*

Nanoelectromechanical (NEM) relays can achieve immeasurably low off-state leakage and can be operated with much lower voltage swing than any transistor. These devices are therefore excellent

candidates for emerging Internet of Things (IoT) applications. Current research aims to demonstrate reliable room-temperature operation of relay-based digital integrated circuits at 10 mV. Key scientific questions that will need to be answered along the way include: 1) What is the fundamental lower limit of operating voltage for mechanical computing? 2) What are key properties of the optimal contact material for milli-Volt mechanical computing? Furthermore, reliable sub-25 mV switching operation of NEM relays was achieved at temperatures below 100 Kelvin. Currently, operation of relays and integrated circuits at temperatures below 1 Kelvin are explored. The goal is to evaluate their compatibility with milli-Kelvin temperatures required for quantum computing.

**Cryo-Photonic WDM Links**

*(Prof. Vladimir Stojanović)*

This project aims to design the photonic links that connect superconducting cryo circuits to the outside environment. Superconducting circuits produce signals with 2-4mV amplitudes, which are then converted to optical signals via CMOS pre-amplifier integrated with specialized ring resonator modulators. The link architecture (Coherent Ultrafast Reflective Link - CURL) is a highly asymmetric link to minimize the thermal dissipation in the cryo environment.

**Quantum Photonics in CMOS**

*(Prof. Vladimir Stojanović)*

In this project, platform building blocks for the photonic quantum computing are being designed as electronic-photonic systems-on-chip. One of the most complex blocks is the photon pair source that produces correlated photon pairs (through laser modulation and nonlinear filtering) that are used as qubits in linear mixing operations.[SI12] The Stojanović group is also working on developing APDs in the same process for detection of the photon pairs for computation read-out.

## 2.6.3 Publications (System Integration – SI)


SI1. K. Settaluri, C. Lalau-Keraly, E. Yablonovitch, and V. Stojanović, "First Principles Optimization of Opto-Electronic Communication Links," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 5, pp. 1270-1283, May 2017.

SI2. F. Chen, H. Kam, D. Markovic, T.J. King Liu, V. Stojanovic, and E. Alon, "Integrated Circuit Design with NEM Relays," *Proc. IEEE/ACM ICCAD*, pp. 750-757, Nov 2008.

SI3. Z. A. Ye, S. Almeida, M. Rusch, A. Perlas, W. Zhang, U. Sikder, J. Jeon, V. Stojanović and T.-J. K. Liu, "Demonstration of Sub-50 mV Digital Integrated Circuits with Microelectromechnical Relays," *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec 2018.

SI4. A.H. Atabaki *et al.*, "Integrating Photonics with Silicon Nanoelectronics for the Next Generation of Systems on a Chip," *Nature*, vol. 556, pp. 349-354, Apr. 2018.

SI5. B. Yin, H. Gevorgyan, D. Onural, A. Khilo, M. A. Popović, and V. M. Stojanović, "Electronic-Photonic Cryogenic Egress Link," *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, pp. 51-54, Sep 2021.

SI6. U. Sikder, K. Horace-Herron, T.-T. Yen, G. Usai, L. Hutin, V. Stojanović, and T.-J. King Liu, "Toward Monolithically Integrated Hybrid CMOS-NEM Circuits," *IEEE Transactions on Electron Devices*, vol. 68, pp. 6430-6436, Dec 2021.

SI7. L. P. Tatum, U. Sikder, and T.-J. K. Liu, "Design Technology Co-Optimization for Back-End-of-Line Nonvolatile NEM Switch Arrays," *IEEE Transactions on Electron Devices*, vol. 68, pp. 1471-1477, Apr 2021.

SI8. C. Adamopoulos, S. Buchbinder, P. Zarkos, P. Bhargava, A. Gharia, A. Ninkejad, M. Anwar, and V. Stojanovic, "Fully Integrated Electronic-Photonic Sensor for Label-Free Refractive Index Sensing in Advanced Zero-Change CMOS-SOI Process," *2021 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-2, May 2021.

SI9. P. Zarkos, S. Buchbinder, C. Adamopoulos, S. Madhvapathy, O. Hsu, J. Whinnery, P. Bhargava, and V. Stojanović, "Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Imaging Applications in a Zero-Change 45nm CMOS-SOI Process," *2021 Symposium on VLSI Circuits*, pp. 1-2, Jun 2021.

SI10. C. Adamopoulos, S. Buchbinder, P. Zarkos, P. Bhargava, A. Gharia, A. Niknejad, M. Anwar, and V. Stojanović, "Fully Integrated Electronic–Photonic Biosensor for Label-Free Real-Time Molecular Sensing in Advanced Zero-Change CMOS-SOI Process," *IEEE Solid-State Circuits Letters*, vol. 4, pp. 198-201, Nov 2021.

SI11. C. Adamopoulos, P. Zarkos, S. Buchbinder, P. Bhargava, A. Niknejad, M. Anwar, and V. Stojanović, "Lab-on-Chip for Everyone: Introducing an Electronic-Photonic Platform for Multiparametric Biosensing Using Standard CMOS Processes," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 1, pp. 198-208, Oct 2021.

SI12. J. M. F. Cabanillas, D. Kramnik, A. Ramesh, C. M. Gentry, V. Stojanović, P. Kumar, and M. A. Popović, "Tunable Source of Quantum-Correlated Photons with Integrated Pump Rejection in a Silicon CMOS Platform," in *Frontiers in Optics + Laser Science 2021*, C. Mazzali, T. (T.-C.) Poon, R. Averitt, and R. Kaindl, eds., *Technical Digest Series (Optica Publishing Group, 2021)*, paper FTu2E.1, Nov 2021.

## 2.7 Computational Imaging

*Research activities of the Computational Imaging/Metrology Thrust have been supported in part by directed membership contributions of **Lam Research**.*

Computational imaging is an emerging field of metrology, involving the co-design of imaging system hardware and software for optimization across the entire pipeline from acquisition to reconstruction. The defining idea is that computers can replace bulky and expensive optics by solving computational inverse problems. With this approach, new, computational-imaging-based microscopes can be designed for 3D aberration and phase measurement. Computational imaging research in the BETR Center is led by **Professor Laura Waller**, and it is focused on designing imaging systems and algorithms jointly using simple hardware, which is easily adoptable and advanced image reconstruction algorithms based on large-scale optimization and learning. The **Waller** group is also exploring a new direction in computational imaging by not just reconstructing images from a given data set but encoding the information in the hardware and using data-driven approaches to optimize capture of the images and set up of the physical system in conjunction with image reconstruction.[CI1] Past projects, for example, focused on a feasibility study for transferring optical phase measurements for inspection of large optical components in the supply chain of BETR Center industrial affiliate **Lam Research.** The team is also conducting fundamental research in the field of EUV lithography that could be applied to various semiconductor applications, including probing thin-film structures to sub-atomic length-scales,[CI2] measuring phase of EUV masks for lithographic imaging,[CI3] and investigating next-generation designs for EUV photomasks.[CI4]

### 2.7.1 Recent Achievements

*A. Learned Adaptive Multiphoton Illumination Microscopy*

In recent year, multiphoton microscopy has emerged as a powerful technique for deep in vivo imaging in scattering samples. However, it requires precise, sample-dependent increases in excitation power with depth to generate contrast in scattering tissue, while minimizing photobleaching and phototoxicity. While adaptive optics and adaptive illumination techniques provide some improvement, they still result in increased photobleaching when imaging curved or irregularly shaped samples. In this period, the **Waller** group introduced an entirely new, data-driven technique approach, which shows how adaptive imaging can optimize illumination power at each point in a 3D volume as a function of the sample's shape, without the need for specialized fluorescent labeling.[CI5] This method can provide 10-100x increase in the volume to which appropriate illumination power can be applied in curved samples such as lymph nodes, and a reproducible way to automatically apply the minimal illumination needed to observe structures of interest, thereby conserving the photon budget and minimizing the perturbation to the sample induced by the imaging process.

The new method, called learned adaptive multiphoton illumination (LAMI), relies on using a one-time calibration experiment to learn the parameters of a physics-based machine learning model

that captures the relationship between fluorescence intensity and incident excitation power in a standardized sample, given the sample's shape. On subsequent experiments, this enables continuous adaptive modulation of incident excitation light power as a focal spot is scanned through each point in the sample. Importantly, only a simple hardware modification to an existing multiphoton microscope is needed to enable modulation of laser power as the excitation light is scanned throughout the sample, costing less than $50 for most modern multiphoton systems. The team used this technique for in vivo imaging of immune responses in mouse lymph nodes following vaccination (Figure 19). After a one-time calibration experiment, the trained neural network could be used to automatically modulate excitation power to the appropriate level at each point in new samples, enabling dynamic imaging of the immune system with single-cell resolution across volumes of tissue more than an order-of-magnitude larger than previously described. They achieved visualization of physiologically realistic numbers of antigen-specific T cells (~2 orders of magnitude lower than previous studies) and demonstrated changes in the global organization and motility of dendritic cell networks during the early stages of the immune response. These first experiments confirm that LAMI is a powerful technique for adaptive illumination in multiphoton imaging, with the potential for opening a range of biological investigations.

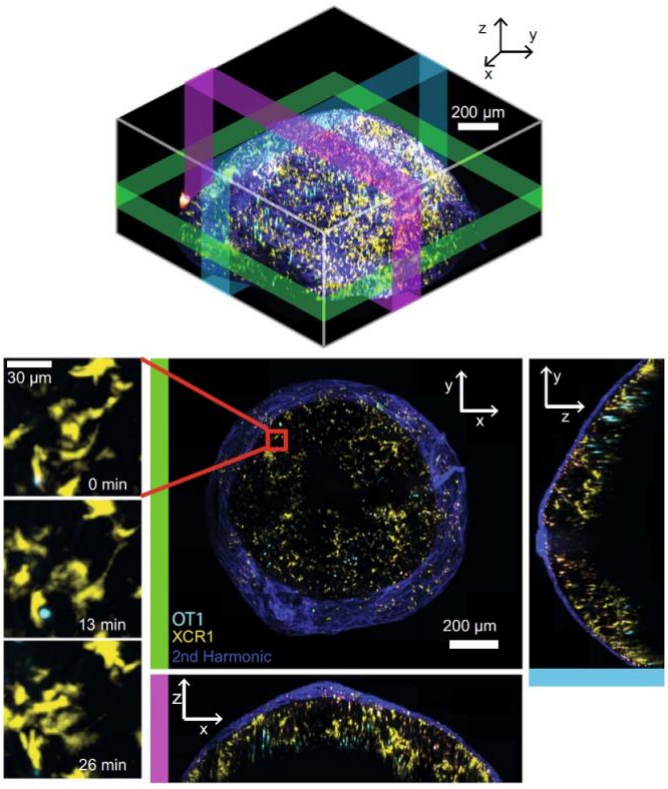



**Figure 19. Top.** Dendritic cell clustering, visualized and quantified on the whole lymph node level. 3D view with colored bars marking areas shown in 2D projections below. **Bottom.** XY, YZ, XZ projections with zoomed-in area show an example of dendritic cell cluster forming over 26 min.

### *B. Picometer Sensitivity Metrology for EUV Absorber Phase*

EUV attenuated phase shift masks have attracted considerable interest due to their superior image quality for applications such as dense contact and pillar arrays. With this growing interest, it has become critical to model, measure, and monitor the relative intensity and phase of multilayer and absorber reflections. The **Waller** group developed a solution based on physical modeling of reflectometry data, which is capable of achieving single picometer phase precision by characterizing the phase of an EUV photomask via measurements of reflectivity from multilayer and absorber regions (Figure 20).[CI2] The group derived a 28-parameter physical model, which was used to extract the effective propagation distance for each reflection coefficient in both regions.

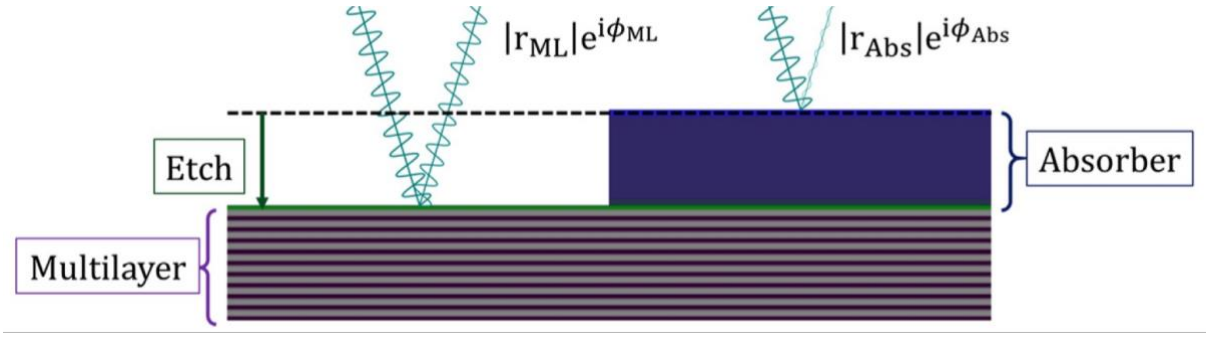



**Figure 20.** Schematic depiction of reflections from absorber and multilayer. Absorber layers from top to bottom are: TaON-Ta-Ru-(Si-MoSi-Mo-MoSi)x40. Multilayer uses same film-stack, with an additional etch depth parameter to replace etched layers with vacuum. An additional C layer is added on top of the absorber, representing hydrocarbon contamination.

They also found that the absorber reflectivity changes systematically from one measurement to the next, unlike the multilayer which displayed changes during storage, but not during exposure. This was attributed to hydrocarbon contamination. Although these changes amount to only a fraction of an atomic monolayer, it was possible to determine the average thickness across the beam-spot to sub-atomic precision. The measurement precision was estimated to be 3-4 pm in terms of the 13.5 nm wavelength.

### *C. Compressive Lensless Photography*

Compressive lensless imagers enable novel applications in an extremely compact device, requiring only a phase or amplitude mask placed close to the sensor. This imaging technique aims to recover more samples than measured by leveraging compressive sensing, which guarantees signal recovery for underdetermined systems given certain assumptions about signal sparsity as well as incoherence in the measurement domain. Typically, this is accomplished by using convex optimization and hand-picked priors, or by deep learning-based reconstruction methods. The latter are better but require many thousands of ground truth training pairs, which can be difficult or impossible to acquire. The **Waller** group proposed a reconstruction method for compressive lensless imaging based on untrained networks—called untrained deep network (UDN) reconstructions—which uses a deep network for the image prior but requires no training data (Figure 21).[CI6]

The team demonstrated that untrained networks could improve the image quality for lensless compressive imaging systems by testing untrained networks on 2D lensless imaging with varying amounts of erasures. They also demonstrated the effectiveness on single-shot compressive video and single-shot hyperspectral imaging, in which they recovered a full 72-frame video or 32 to 64 spectral slices, respectively, from a single measurement. In each case, the team showed that both in simulation and experiment untrained networks can have better image quality than compressive-sensing-based minimization using total-variation regularization, demonstrating that non-linear networks can be a better prior than TV for dense, natural scenes. Untrained networks are especially promising for situations in which training data is difficult or impossible to obtain, providing a better imaging prior for underdetermined reconstructions.

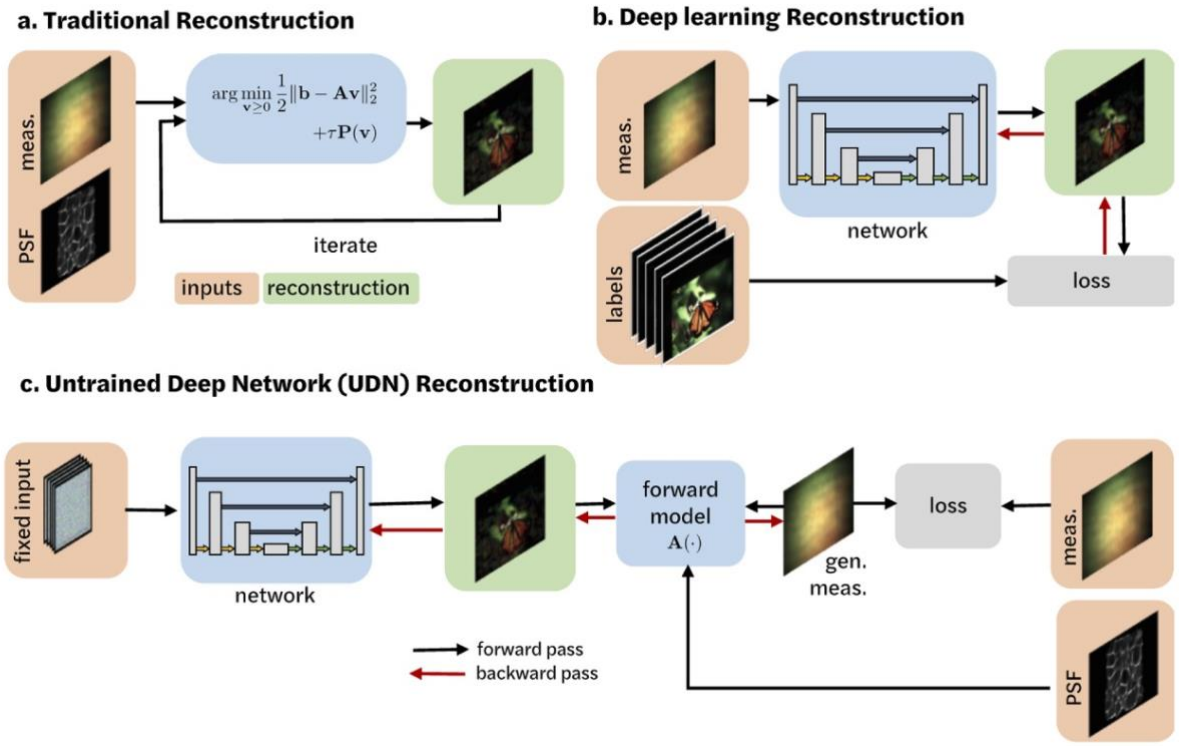



**Figure 21.** Comparison of different reconstruction approaches. **a)** Traditional reconstructions solve a convex optimization problem with a data-fidelity-term based on the known forward model and a regularization term which acts as the image prior. **b)** Deep learning methods require thousands or more labeled image pairs to train a neural network to approximate the reconstruction. **c)** The untrained deep network (UDN) uses a neural network as the image prior but does not require any training data. The system forward model is used to calculate the loss between the estimated image and the measurement, which is then used to update the network weights.

## 2.7.2 Current Projects

### Computational Microscopy for EUV Applications

*(Prof. Laura Waller)*

The Waller group is working on computational microscopy techniques applied to EUV and optical metrology. For example, they can use custom partially coherent illumination patterning and computational inverse problems, or phase masks in the pupil plane, to accurately recover the wavefront phase delays to a fraction of a wavelength, thus giving morphological measurements for masks and potentially wafer-level features. These methods offer resolution well beyond the diffraction limit imposed by the imaging system's numerical aperture, along with a large field-of-view for large-scale metrology applications.

## 2.7.3 Publications (Computational Imaging – CI)

CI1. L. Waller, "Computational Phase Microscopy," *Proc. SPIE, Biophotonics and Biomedical Microscopy*, vol. 11575, pp. 1157502, Oct 2020.

CI2. S. Sherwin, I. Cordova, R. Miyakawa, M. Benk, L. Waller, A. Neureuther, and P. Naulleau, "Picometer Sensitivity Metrology for EUV Absorber Phase," *J. Micro/Nanopattern. Mats. Metro.*, vol. 20, p. 031011, Aug 2021.

CI3. S. Sherwin, R. Miyakawa, M. Benk, L. Waller, A. Neureuther, and P. Naulleau, "Measuring EUV Mask 3D Effects with Hyperspectral Zernike Phase Contrast," *Proc. SPIE, Extreme Ultraviolet (EUV) Lithography XII*, vol. 11609, pp. 116090B, Mar 2021.

CI4. S. Sherwin, L. Waller, A. Neureuther, and P. Naulleau, "Advanced Multilayer Mirror Design to Mitigate EUV Shadowing," *Proc. SPIE, Extreme Ultraviolet (EUV) Lithography X*, vol. 10957, pp. 1095715, Mar 2019.

CI5. H. Pinkard, H. Baghdassarian, A. Mujal, E. Roberts, K. H. Hu, D. H. Friedman, I. Malenica, T. Shagam, A. Fries, K. Corbin, M. F. Krummel, and L. Waller, "Learned adaptive multiphoton illumination microscopy for large-scale immune response imaging," Nature Communications, vol. 12, p. 1916, Mar 2021.

CI6. K. Monakhova, V. Tran, G. Kuo, and L. Waller, "Untrained Networks for Compressive Lensless Photography," *Opt. Express*, vol. 29, pp. 20913-20929, Jun 2021.

## 2.8 Optical Interconnects and Integration

Silicon photonics technology is rapidly being adopted for high-speed communication between servers within data centers because optical signals can propagate faster and with better energy efficiency than voltage signals. Light also can be used to transmit data across a chip, through silicon microstructures which act as waveguides. However, significant improvements in the efficiency of miniature light emitters (lasers or light-emitting diodes, LEDs) and in the sensitivity of photodetectors are needed for optical interconnects to be more energy-efficient than electrical interconnects; the state of the art is hundreds of fJ/bit, orders of magnitude greater than the quantum limit of 20 aJ/bit. BETR Center researchers from the groups of **Professors Ali Javey**, **Vladimir Stojanović**, **Ming Wu**, and **Eli Yablonovitch** are addressing these needs by investigating the incorporation of optical antennas to enhance the spontaneous emission rate of LEDs, and by exploring novel approaches to alleviate tradeoffs between photodetector speed, capacitance, and optical absorption.[OI1-OI3] This research entails innovation of new optoelectronic device concepts, integration of advanced materials, and IC design breakthroughs to increase the communication bandwidth of silicon photonic chips.

### 2.8.1 Recent Achievements

*A. High-Efficiency Metal-Dielectric Optical Antennas*

The optical antenna-LED was invented in the Center for E$^3$S by **Yablonovitch** and **Wu**. It is a new light source with great promise for energy-efficient on-chip optical communication because it can produce spontaneous emission enhancements of more than 200 times under electrical excitation.[OI1] At its core is a metal antenna, which spontaneous emission of an oscillating dipole can couple to, thereby increasing its steady-state radiation power. However, one finds that the large enhancement factor of spontaneous emission comes at the expense of inefficiency in metallic optical antennas because of Ohmic losses and nonlocal surface collision effects.

In this period, the **Yablonovitch** and **Wu** groups developed a new metal-dielectric antenna design (Figure 22a), which eliminates the tradeoff between spontaneous emission enhancement and

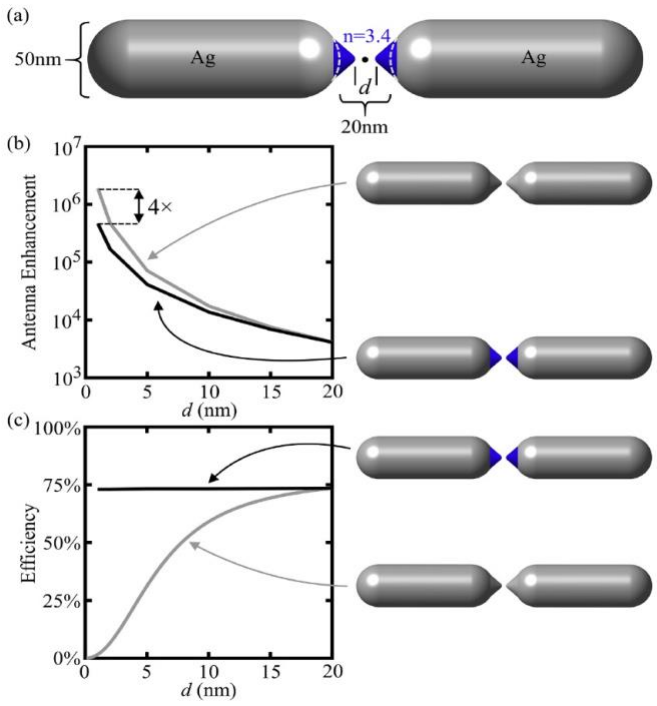



**Figure 22. a)** Metal-dielectric dipole antenna with sharp dielectric tips (blue). **b, c)** FDTD calculation of the enhancement **(b)** and efficiency **(c)** of the metal-dielectric antenna (black line) and the all-metal antenna (silver line) as a function of *d* at a wavelength of λ = 1550 nm.

radiative efficiency by using nanoscopic dielectric structures at the antenna tips.[OI4] The team found that these metal-dielectric antennas can enhance spontaneous emission by a factor of $5x10^5$ with efficiencies of ~70%. This greatly exceeded the radiative efficiency of a purely metallic antenna with similar enhancement (Figure 22b and c). Moreover, the metal-dielectric antenna design strategy is naturally amenable to short-distance optical communications applications and can be integrated into an optical antenna-LED design.

### *B. Tunable IR Optoelectronics with Black Phosphorus*

Room-temperature optoelectronic devices that operate at a wide range of infrared wavelengths (one to eight micrometers) are important for numerous optoelectronic devices, including LEDs and photodetectors. To achieve the range of operating wavelengths, a combination of materials with different bandgaps or variations in the composition of semiconductor alloys during growth are used. However, these materials are difficult to fabricate, and the operating range is fixed after fabrication. In contrast, the **Javey** group developed high-performance room-temperature infrared optoelectronics with actively variable spectra using black phosphorus as active component.[OI5] Using the highly strain-sensitive nature of the bandgap of black phosphorus (Figure 23a and b), which varies from 0.22 to 0.53 eV, the team demonstrated a continuous and reversible tuning of the operating wavelengths in black phosphorus–$MoS_2$ light-emitting diodes (Figure 23c-d) and photodetectors.

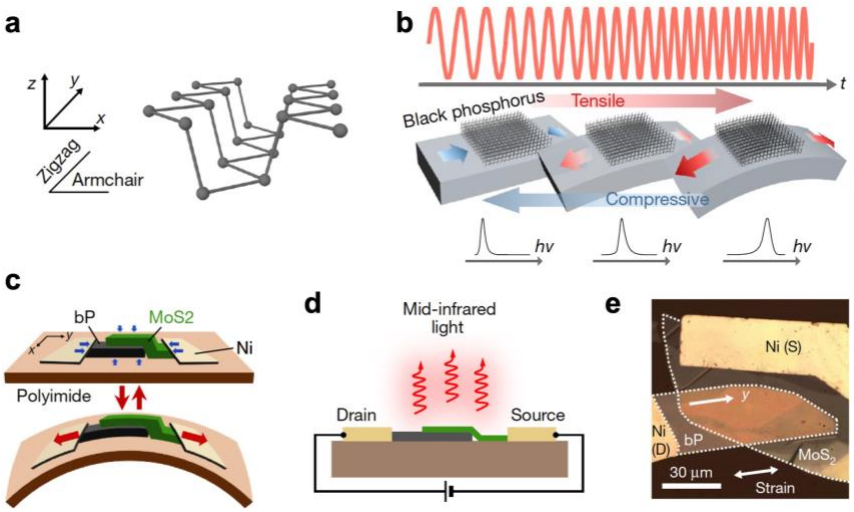



**Figure 23.** Strain-tunable bandgap in black phosphorus. **a)** Schematic illustrating the anisotropic crystal structure of black phosphorus along the armchair and zigzag directions. **b)** Schematic representation of the strain-induced actively tunable bandgap of black phosphorus. Compressive and tensile strains induce redshift and blueshift of the black phosphorus bandgap, respectively. **c)** Schematic showing a strain-tunable black phosphorus–$MoS_2$ LED. **d)** Schematic of the device architecture, showing mid-infrared electroluminescence under forward bias across the phosphorus–$MoS_2$ heterojunction on a polyimide substrate. **e)** Optical micrograph of a representative device.

Furthermore, the **Javey** group leveraged this platform to demonstrate multiplexed nondispersive infrared gas sensing, whereby multiple gases (for example, carbon dioxide, methane, and water vapor) are detected using a single light source. The actively variable-spectrum optoelectronic (AVSO) devices developed in this project have unprecedented versatility and thus important implications in fields such as optical communications, chemical sensing, and spectroscopy, where a tunable spectrum is required. This active strain-tuning scheme might also be applicable to other 2D materials, providing a path towards spectrally tunable optoelectronics across the electromagnetic spectrum.

*C. 2D Random-Access Optical Beam Steering System*

The **Wu** group developed a two-dimensional random-access optical beam steering system.[OI6] Such devices are the key components for many applications, including light detection and ranging (LiDAR) and free-space optical communications. Integrated beam steering devices with fast steering speed, low power consumption and large field-of-view (FoV) are highly demanded to address the drawbacks of their bulky mechanical counterparts. Opt-ical phased arrays have been demons-trated for 2D beam steering, however, they require precise control of thousands of phase shifting elements at the same time.

The optical beam steering system originally introduced by the **Wu** group is much simpler and is composed of a 20×20 focal plane switch array integrated on a silicon photonics chip with microelectromechanical-system (MEMS) optical switches. In this period, the group demonstrated a new design with a much larger 128×128-element two-dimensional silicon photonics focal plane (Figure 24).[IO7] The new device has a switch array with row-column addressing, random-access 2D beam steering with a 70°×70° field-of-view with a 0.6°×0.6° resolution, a beam divergence of 0.050°×0.049°, and sub-MHz steering speed. This device is a promising candidate for integrated LiDAR and FSOC systems, and it can be further improved by increasing the chip size, shrinking the array pitch, selecting a wide-angle lens, and optimizing the grating antennas.

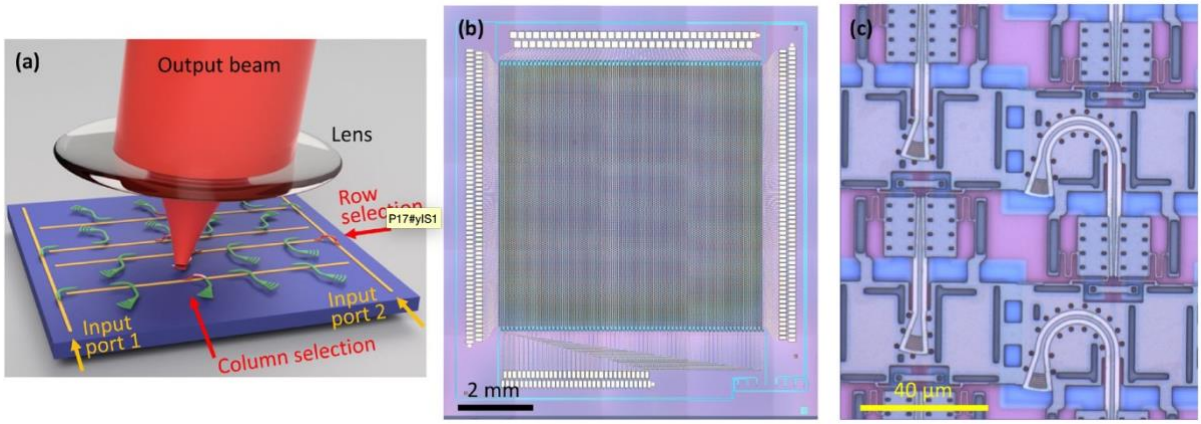



**Figure 24. a)** Schematic of the beam steering system with a 4×4 FPSA. The switches and grating antennas in the ON state are colored in red. The MEMS actuators are not shown in the schematic for clarity. **b)** Microscopic image of the fabricated 128×128 FPSA on a 10×11 $mm^2$ chip. **c)** Microscopic image showing the MEMS optical switches and grating antennas.

## 2.8.2 Current Projects

**Silicon Photonic Super-Switch**

*(Prof. Ming Wu)*

The goal of this project is to develop large-scale silicon photonic switches (1000x1000) with fast response time (microsecond) and low optical loss (3dB fiber-to-fiber). This project has 3 tasks: Task 1 will develop scalable silicon photonic MEMS technology with super low loss. Task 2 will

develop custom CMOS ASICs that will be directly flip-chip integrated on Si photonic switch for digital control. Task 3 will develop array fiber packaging technology with low insertion loss (< 0.5 dB). The team is currently in Phase 1 whose goal is to demonstrate 128x128 silicon photonic switch with integrated CMOS control and 8 dB fiber-to-fiber loss.

**Development of Ultrafast LEDs**

*(Prof. Ali Javey)*

The Javey group has identified a novel material based on molecular monolayers that exhibits near 100% photoluminescence quantum yield with a radiative lifetime of only 10 psec. The switching speed of a LED is limited by the carrier lifetime. For efficient/bright LEDs, a typical lifetime today is at best on the order of 10's of nsec. That limits how fast they can be switched. The team aims to use this new material class to make efficient LEDs with 10's of psec switching time. They have studied materials physics and now want to build devices to prove the concept.
*(Recent publication: Zhao et al., "Strong optical response and light emission from a monolayer molecular crystal", Nature Communications, 10, 5589, 2019)*

**Efficient LEDs Based on Defect-Tolerant Materials**

*(Prof. Ali Javey)*

Previously, the Javey group observed that for transition metal dichalcogenide (TMDC) monolayer semiconductors (e.g., MoS2, WS2, WSe2) there was a sharp drop in photoluminescence quantum yield (PLQY) at high exciton concentrations due to exciton-exciton annihilation (EEA), which is non-radiative. This was a major limitation for the use of monolayers in efficient practical devices. Recently (unpublished), they showed that EEA is resonantly amplified in TMDC monolayers by van Hove singularities (VHSs) present in their joint density of states. Logarithmic VHSs are a hallmark of two-dimensional semiconductors. By applying small mechanical strain (~0.2%), the EEA process is shifted away from the VHS resonance and circumvent the enhanced nonradiative EEA that plagues the PLQY at high exciton densities, leading to near-unity PLQY at all exciton densities in 2D TMDC monolayers. Combined with counterdoping, this simple method suppresses all nonradiative recombination at all generation rates for both exfoliated and CVD-grown centimeter-scale TMDC monolayers. The group has studied materials physics and is now ready to build devices to prove the concept.

**Compact Fourier Transform Infrared Spectrometer on Chip**

*(Prof. Ming Wu)*

The goal of this project is to investigate and prototype chip-scale Fourier-Transform Infrared (FTIR) spectrometer enabled by low-loss silicon photonic micro-electro-mechanical-system (MEMS) switches and on-chip delay lines.

**Variable Spectrum Optoelectronics**

*(Prof. Ali Javey)*

Some 2D semiconductors exhibit a large band structure modulation by strain, larger than what is seen in classical systems. Furthermore, they can inherently tolerate larger strain values due to

crystal structure. Taking advantage of these features, the Javey group has recently built actively variable spectrum LEDs and photodetectors for which a single device shows wavelength tunability from ~0.2 to 0.5 eV by applying a mechanical strain. It's effectively a MEMs device and by tuning the strain, the emission or absorption peak can be actively tuned from LWIR to mid-IR (unpublished, recently submitted). The group is exploring opportunities for various applications including spectroscopy.

**Photonically-Remoted Endoscopic Ultrasound Array**

*(Prof. Vladimir Stojanović)*

The Stojanović group is developing an ultrasound array readout beamforming system that consists of the low-power ring-resonator ultrasound sensor array chip (with thousands of sensors in an ultrasound probe integrated with ring thermal tuners) with a companion remoted receiver array chip. The ultrasound sensing capability of the ring resonator array opens the new applications beyond endoscopic ultrasound, such as photoacoustic imaging.

**Photonic Label-Free Molecular Sensing**

*(Prof. Vladimir Stojanović)*

The Stojanović group is using ring-resonators with integrated read-out circuits as molecular and viral nanoparticle sensors, developing the point-of-care and potentially implantable single-chip platforms for multi-analyte label-free sensing. Example application - multi-analyte (virus and antibody detection point-of-care testing for Covid-19).

## 2.8.3 Publications (Optical Interconnects – OI)


OI1. S. A. Fortuna, A. Taghizadeh, E. Yablonovitch, and M. C. Wu, "Toward 100 GHz Direct Modulation Rate of Antenna Coupled NanoLED," *IEEE Photonics Conference*, Jan 2016.

OI2. K. Settaluri, C. Lalau-Keraly, E. Yablonovitch, and V. Stojanović, "First Principles Optimization of Opto-Electronic Communication Links," IEEE Transactions on Circuits and Systems I: Regular Papers , vol.64, no.5, pp. 1270-1283, May 2017.

OI3. D.-H. Lien, M. Amani, S.B. Desai, G.H. Ahn, K. Han, J.-H. He, J.W. Ager, M.C. Wu, and A. Javey, "Large-Area and Bright Pulsed Electroluminescence in Monolayer Semiconductors," *Nature Communications*, vol. 9, pp. 1229, Mar 2018.

OI4. S. Hooten, N. M. Andrade, M. C. Wu, and E. Yablonovitch, "Efficient Spontaneous Emission by Metal-Dielectric Antennas; Antenna Purcell Factor Explained," *Opt. Express*, vol. 29, pp. 22018-22033, Jul 2021.

OI5. H. Kim, S. Z. Uddin, D.-H. Lien, M. Yeh, N. S. Azar, S. Balendhran, T. Kim, N. Gupta, Y. Rho, C. P. Grigoropoulos, K. B. Crozier, and A. Javey, "Actively Variable-Spectrum Optoelectronics with Black Phosphorus," *Nature*, vol. 596, pp. 232-237, Aug 2021.

OI6. X. Zhang, K. Kwon, J. Henriksson, J. Luo, and M.C. Wu, "A 20×20 Focal Plane Switch Array for Optical Beam Steering," *2020 Conference on Lasers and Electro-Optics (CLEO)*, San Jose, CA, pp. 1-2, Sep 2020.

OI7. X. Zhang, K. Kwon, J. Henriksson, J. Luo, and M. C. Wu, "Large-scale Silicon Photonics Focal Plane Switch Array for Optical Beam Steering," *Optical Fiber Communication Conference (OFC) 2021*, paper F4A.2, Jun 2021.

# 3. Knowledge Transfer

## 3.1 Overview

Knowledge transfer is at the heart of the BETR Center's mission of fostering groundbreaking discoveries and fertilizing new technologies. In the BETR Center, knowledge transfer is seen as a two-way street: Sharing the latest research outcomes of BETR with various stakeholders, while bringing new knowledge into the Center by engaging with its industry affiliate members and other key players in semiconductor technologies.

In fact, the BETR Center was established with the recognition that partnerships with leading semiconductor companies are a key factor in accelerating research, education and outreach endeavors. Since then, the Center has put significant efforts into sharing new knowledge with industry, academia and research labs. Interactions have taken place at various levels, including seminars/webinars by internal and external speakers, visits and customized briefings (online or in-person) for BETR Center industry affiliates, and biannual BETR Center workshops.

Additional knowledge transfer vehicles used by the BETR Center for sharing new discoveries with the wider research community are publications in scientific journals and conferences proceedings, as well as patents and invention disclosures. To that end, twice a year, the BETR Center shares a list of research publications (including copies of published papers) and patent applications with all industry affiliates. Moreover, if requested by an industry affiliate, technology licensing will be facilitated by introductions to the UC Berkeley Industry Alliances Office and Office of Technology Licensing.

Finally, the BETR Center recognizes that education itself is an important knowledge transfer element by preparing the Center's students and postdoctoral researchers to be the next-generation leaders in physical electronics and semiconductor technologies. The BETR Center facilitates interaction of Center students and postdocs with representatives of its industry affiliates through seminars/webinars, poster sessions at the biannual BETR Center Workshops, and targeted recruiting events (upon request by industry affiliates). Furthermore, the Center has been working with industry affiliates in identifying BETR Center students and postdocs for various internship positions.

In the following, detailed information about activities in the last year in BETR Center's four main knowledge transfer areas are provided:

- BETR Center Workshops
- Solid State Technology and Devices Seminars/Webinars
- Publications in Scientific Journals and Conference Proceedings
- Intellectual Property and Invention Disclosures

## 3.2 BETR Center Workshops

The workshops of the BETR Center, held twice annually, are prime knowledge transfer opportunities, connecting faculty, postdocs and students of the Center with representatives of its industry affiliates and other invited companies from the semiconductor industry. While these workshops were traditionally held as in-person events, restrictions due to the COVID pandemic forced us to hold the two 2021 workshops as online events. Workshops feature oral presentations from BETR Center researchers, lightning talks and a poster session by the Center's students and postdocs, as well as industry panels and broad discussion forums about the latest technology trends and challenges. In addition, all workshops include a one-hour closed session between the BETR Center leadership and members of the Technical Advisory Board (with representatives from all industry affiliates).

All workshop presentations are recorded and made available to industry affiliates on the BETR Center website (https://betr.berkeley.edu). Note that a BETR Center website account (with unique username/password) is needed to access the recordings. BETR Center website accounts may be requested by representatives of industry affiliates by email to betr@berkeley.edu.

### Spring 2021 Workshop

The Spring 2021 Workshop of the BETR Center was held as a two-day online event on May 27-28, 2021 (see Appendix B for the full workshop agenda). The workshop was attended by 69 participants, including 22 BETR Center students and postdocs and 36 representatives from industry. It featured seven talks by BETR Center co-directors, postdocs and students, and 13 student/postdoc lightning talks, followed by a virtual poster session. The Spring Workshop had also a student-moderated panel about "Current Trends, Opportunities and Challenges in the Semiconductor Industry" with the following panelists: **Dr. Carlos Diaz** (TSMC), **Dr. Philip Kraus** (Applied Materials), and **Dr. Ben Haskell** (Lam Research).

Representatives of the following BETR Center industry affiliates participated in the closed session meeting of the Technical Advisory Board with BETR Center Leadership: **Applied Materials**, **Lam Research**, **TSMC**, and the new BETR Center member **Intel Corporation**.

*Talks by BETR Center co-Directors, Students, and Postdocs*

- **Ramamoorthy Ramesh:** "Electric Field Control of Magnetism for Beyond CMOS Electronics"
- **Urmita Sikder:** "Towards Monolithically Integrated Hybrid CMOS-NEM Circuits"
- **Yuxuan Cosmi Lin:** "Towards Ultimately Scaled Transistors with Low-Dimensional Materials"
- **Eli Yablonovitch:** "Onsager Computing versus Quantum Computing"

- **Sayeef Salahuddin:** "Ising Computing: Compositional Training and Parallel Asynchronous Sampling"
- **Ana Arias:** "Printed Flexible Sensors"
- **Laura Waller:** "Computational Imaging for Metrology"

*Lightning Talks and Posters by BETR Center Students and Postdocs*

- **Hyungjin Kim** (Javey group): "Actively Tunable Midwave/Longwave IR Emitters and Detectors"
- **Christos Adamopoulos** (Stojanović group): "Fully Integrated Electronic-Photonic Biosensor for Label-Free Molecular Sensing in Advanced Zero-Change CMOS-SOI Process"
- **Anju Toor** (Arias group): "Printed Miniaturized Li-ion Batteries for Autonomous Microsystems"
- **Emma Wawrzynek** (Arias group): "Printed Biodegradable IDE Capacitor for Humidity Monitoring"
- **Stuart Sherwin** (Waller group): "Picometer Phase Metrology for EUV Masks"
- **Payton Goodrich** (Arias group): "Naturally Degradable Nitrate Sensors for Precision Agriculture"
- **Hanuman Singh** (Bokor group): "Generation of Picosecond Current Pulse with Auston Switch on Arbitrary Substrate Using Layer Transfer Technique"
- **Xiaoer Hu/Lars Tatum** (Liu group): "Self-Oscillation of MEM Relays"
- **Philip Jacobson** (Wu group): "Hybrid Reservoir Computing for Image Recognition"
- **Sucheta Mondal** (Bokor group): "Antiferromagnetic Switching in NiO/Pt Bilayers with Large Domains"
- **Xiaoxi Huang** (Ramesh group): "Novel spin-orbit torque generation at room temperature in an all-oxide epitaxial La0.7Sr0.3MnO3/SrIrO3 system"
- **Panagiotis Sarkos** (Stojanović group): "Monolithically Integrated Electronic-Photonic Ultrasound Receiver Array"
- **Gautam Gunjala** (Waller group): "EUV microscope characterization using photomask surface roughness"

*Industry Panel Discussion: "Current Trends, Opportunities and Challenges in the Semiconductor Industry"*

- **Urmita Sikder**, UC Berkeley (Moderator)
- **Lars Tatum**, UC Berkeley (Moderator)
- **Carlos Diaz**, TSMC (Panelist)
- **Philip Kraus**, Applied Materials (Panelist)
- **Ben Haskell**, Lam Research (Panelist)

## Fall 2021 Workshop

The Fall 2021 BETR Workshop was again held as a two-day online event on November 15-16, 2021 (see Appendix C for the full workshop agenda). BETR Center co-directors, postdocs, and students gave 10 presentations in addition to 13 student/postdoc lightning talks, which were followed by a virtual poster session. The Fall Workshop also featured an open discussion forum on "Workforce Development" led by BETR co-Director and COE Dean Prof. **Tsu-Jae King Liu**. The workshop was attended by 74 participants, including 21 BETR Center students and postdocs and 41 representatives from industry.

The closed session of the Technical Advisory Board with BETR Center leadership was attended by representatives of BETR Center industry affiliates **Applied Materials**, **Lam Research**, **TSMC**, **Intel Corporation**, and the new BETR Center members **AMD** and **Facebook/Meta**.

*Talks by BETR Center co-Directors*

- **Sophia Shao:** "Next-Generation Deep-Learning Accelerators: From Hardware to System"
- **Xiaoer Hu:** "Study of DC-Driven MEM Relay Oscillators for Implementation of Ising Machines"
- **Pratik Brahma:** "Machine Acceleration of Many-Body Quantum Mechanics"
- **Jeffrey Bokor:** "Graphene Nanoribbon Transistors"
- **Jasmine Jan:** "Flexible Blade-coated Devices: Dual Functionality with Simultaneous Deposition"
- **Anju Toor:** "Printed, Li-ion Miniature Batteries for On-chip Electronics"
- **Ming Wu:** "Reconfigurable Silicon Photonic Integrated Circuits"
- **Vivian Wang:** "Bright Emission Across the Spectrum with a Generic Electroluminescent Device"

- **Stuart Sherwin:** “Improvements in Modeling, Design, and Metrology for EUV Photomasks”
- **Vladimir Stojanović:** “Electronic-Photonic Systems on Chip”

*Lightning Talks and Posters by BETR Center Students and Postdocs*

- **Lucas Caretta** (Ramesh group): “Nonvolatile Electric Field Control of Inversion Symmetry”
- **Eric Parsonnet** (Ramesh group): “Electric Field Control of Thermal Magnons in BiFeO3”
- **Shehrin Sayeed** (Salahuddin group): “Spin-Orbit Torque Rectifier for Weak RF Energy Harvesting”
- **Zafer Mutlu** (Bokor group): “Double-Gate Graphene Nanoribbon FETs”
- **Lars Tatum** (Liu group): “MOSFET Exhibiting Negative Differential Resistance (NDR-FET) for Embedded Memory Applications”
- **Hansung Kim** (Shao group): “Workload Characterization of Ray Tracing”
- **Dima Nikiforov** (Shao group): “A Co-Simulation Platform Enabling the Performance Characterization of Quadrotor SoCs”
- **Emma Wawrzynek** (Arias group): “Characterization and Comparison of Biodegradable Printed Capacitive Humidity Sensors”
- **Payton Goodrich** (Arias group): “Naturally Degradable Nitrate Sensors for Precision Agriculture”
- **Amirmahdi Honardoost** (Wu group): “Low-Loss Wafer-Bonded Silicon Photonic MEMS Switches”
- **Bozhi Yin** (Stojanović group): “Electronic-Photonic Cryogenic Egress Link”
- **Daniel Kramnik** (Stojanović group): “CMOS Quantum Photonics”
- **Gautam Gunjala** (Waller group): “Accuracy of Speckle-based Aberration Measurement in an EUV Microscope”

*Open Forum Discussion: “Workforce Development”*

- **Tsu-Jae King Liu**, UC Berkeley (Presenter & Moderator)
- **Michael Bartl**, UC Berkeley (Moderator)

## 3.3 Solid State Technology and Devices Seminar Series

The BETR Center has continued hosting the *Solid State Technology and Devices Seminar Series* of the UC Berkeley Electrical Engineering and Computer Science department. Solid State Technology and Devices seminars are usually held on Fridays (1:00-2:00 pm Pacific) by invited speakers who are experts from academia, national labs, and industry. Due to ongoing COVID-19 restrictions, almost all seminars were held online. A total of 21 seminars were held in the 2021/2022 reporting period and were simulcast to BETR Center members via Webex.

Seminars are usually recorded (with permission by the speaker) and made available to industry affiliates on the BETR Center website (https://betr.berkeley.edu). Note that a BETR Center website account (with unique username/password) is needed to access the seminar recordings. BETR Center website accounts may be requested by representatives of industry affiliates by email to betr@berkeley.edu.

### 2021/22 Solid State Technology and Devices Seminars

- **Tahir Ghani**, Intel Corporation, "Innovations for Continuation of Moore's Law During Next 10 Years", May 7, 2021
- **Luqiao Liu**, MIT, "Magnonic Spintronics: Toward Spin Wave Based Information Processing", May 14, 2021
- **Sanjay Banerjee**, UT Austin, "Electronics and Spintronics in 2D Materials", September 17, 2021
- **Jenna Campbell**, Freedom Photonics, "High Power Diffraction-Limited Tapered Diode Lasers", October 1, 2021
- **Andrei Faraon**, Caltech, "Towards Optical Quantum Networks Based on Rare-Earth Ions and Nano-Photonics", October 15
- **Eric Fossum**, Dartmouth, "Quanta Image Sensor (QIS), or, Detecting Single Electrons in Silicon at Room Temperature, Without Avalanche Multiplication, in a Commercial Product", October 22, 2021
- **John Rogers**, Northwestern, "Transient Electronics", October 29, 2021
- **Walid Redjem**, UC Berkeley, "Color Center in Silicon: From Ensembles to Single Qubit", November 5, 2021
- **Madhavan Swaminathan**, Georgia Tech, "Advanced Packaging, Heterogeneous Integration, and the Future of Semiconductor Systems", November 8, 2021

- **Zafer Mutlu**, UC Berkeley, "High Performance Graphene Nanoribbon Transistors", November 12, 2021
- **Paul McEuen**, Cornell, "Microscopic Robots", November 19, 2021
- **Rutger Vrijen**, McKinsey & Company, "Critical Demand and Supply Trends in Semiconductors", December 12, 2021
- **Miloš Popović**, Boston University, "Convergence of Electronics and Photonics in CMOS Integrated Systems", February 18, 2022
- **Aydogan Ozcan**, UCLA, "Diffractive Optical Networks & Computational Imaging Without a Computer", March 4, 2022
- **Victor Moroz**, Synopsys Inc., "Advanced Logic Technology: Trends and Challenges", March 11, 2022
- **Hui Cao**, Yale University, "Multimode Fiber Optics and Applications", March 18, 2022
- **Ashwin Gopinath**, MIT, "High-Throughput Single-Molecule Assays Using DNA Origami", April 8, 2022
- **Jacob Robinson**, Rice University, "Minimally Invasive Neural Interfaces: Battery-free Bioelectronics and Lensless Microscopes", April 15, 2022
- **Ahmad Bahai**, Texas Instruments, "Innovation in Semiconductors for High Voltage", April 22, 2022
- **Shiekh Zia Uddin**, UC Berkeley, "Understanding Radiative Recombination in Two Dimensional Semiconductors", April 29, 2022
- **Xiaoer Hu**, UC Berkeley, "Micro-Electro-Mechanical Relay Technology for Beyond Von Neumann Architecture", May 6, 2022

More details about the seminars/webinars, including abstract and speaker bio, can be found in Appendix A.

## 3.4 Publications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## 3.5 Technology Transfer

### 3.5.1 Patents and Patent Applications

*US Patent App. 17/252,671*
**Beam-steering System Based on a MEMS-Actuated Vertical-Coupler Array**
X. Zhang, M. C. A. Wu, A. S. Michaels, J. Henriksson
*Application Publ. Date: April 22, 2021*

*US Patent 11,002,953*
**MEMS-based spatial light modulator and method of forming**
Y. Wang, M. C. A. Wu
*Patent Granted Date: May 11, 2021*

*US Patent 11,022,731*
**Optical phase retrieval systems using color-multiplexed illumination**
L. Waller, Z. Phillips, M. Chen
*Patent Granted Date: June 1, 2021*

*US Patent App. 16/768,233*
**Wafer-scale-integrated silicon-photonics-based optical switching system and method of forming**
T. J. Seok, M. C. A. Wu
*Application Publ. Date: June 24, 2021*

*US Patent 11,127,932*
**Simultaneous doctor blading of different colored light emitting components**
A. C. Arias, D. Han, C. M. Lochner, A. Pierre
*Patent Granted Date: September 21, 2021*

*US Patent 11,143,818*
**Multi-mode interference (MMI) based laser devices for heterogeneous platforms**
M. N. Sakib, G. L. Su, J. Heck, H. Rong, M. C. Wu
*Patent Granted Date: October 12, 2021*

*US Patent 11,148,139*
**Microfluidic devices with flexible optically transparent electrodes**
P. Y. E. Chiou, K. W. Huang, I. Y. Khandros, M. C. Wu
*Patent Granted Date: October 19, 2021*

*US Patent App. 17/101,832*

**Printed all-organic reflectance oximeter array**

Y. Khan, D. Han, A. Pierre, J. Ting, X. Wang, C. M. Lochner, A. Arias

*Application Publ. Date: December 23, 2021*

*US Patent App. 17/373,345*

**Pulse oximetry using ambient light**

A. C. Arias, D. Han, Y. T. Khan, J. K. Y. Ting, I. I. Deckman

*Application Publ. Date: February 10, 2022*

*US Patent App. 17/530,863*

**Systems and methods for fabricating conformal magnetic resonance imaging (mri) receive coils**

A. C. Arias, K. Gopalan, A. M. Zamarayeva, M. Z. H. Liu, S. M. Lustig

*Application Publ. Date: March 10, 2022*

*US Patent App. 17/503,999*

**Scalable and High-Performance Pressure Sensors for Wearable Electronics**

A. C. Arias, X. Wu, Y. T. Khan, J. K. Ting, N. A. D. Yamamoto

*Application Publ. Date: May 12, 2022*

### 3.5.2 Available Technologies

*Tech ID: 32471*

**Biodegradable Potentiometric Sensor to Measure Ion Concentration in Soil**

BETR Faculty: Ana Claudia Arias

*Tech ID: 30358*

**Low Band Gap Graphene Nanoribbon Electronic Devices**

BETR Faculty: Jeffrey Bokor, Felix Fischer

*Tech ID: 29091*

**Printed All-Organic Reflectance Oximeter Array**

BETR Faculty: Ana Claudia Arias

*Tech ID: 27270*

**Simultaneous Doctor Blading of Different Colored Organic Light Emitting Diodes**

BETR Faculty: Ana Claudia Arias

*Tech ID: 25799*

**Optical Phase Retrieval Systems Using Color-Multiplexed Illumination**

BETR Faculty: Laura Waller

*Tech ID: 25573*
**Enhancing Photoluminescence Quantum Yield for High Performance Optoelectrics**
BETR Faculty: Ali Javey

*Tech ID: 25105*
**Compressive Plenoptic Imaging**
BETR Faculty: Laura Waller

*Tech ID: 24720*
**System for Patterned Illumination Microscopy**
BETR Faculty: Laura Waller

*Tech ID: 24717*
**Enhanced Patterning of Integrated Circuits**
BETR Faculty: Tsu-Jae King Liu

*Tech ID: 24507*
**Solution Processed Flexible Near-Infrared Organic Light Emitting Diodes and Organic Photodetectors for Wearable Sensors**
BETR Faculty: Ana Claudia Arias

*Tech ID: 24184*
**Chemical-Sensitive Field-Effect Transistor**
BETR Faculty: Ali Javey

*Tech ID: 24171*
**LED array Microscopy Using Multiplexed Illumination Methods and Software**
BETR Faculty: Laura Waller

*Tech ID: 23976*
**Partially Coherent Phase Recovery by Kalman Filtering**
BETR Faculty: Laura Waller

*Tech ID: 23955*
**A Thin Film VLS Semiconductor Growth Process**
BETR Faculty: Ali Javey

*Tech ID: 23488*
**Printed Organic LEDs And Photodetector for A Flexible Reflectance Measurement-Based Blood Oximeter**
BETR Faculty: Ana Claudia Arias

*Tech ID: 23092*

**Micro Electromechanical Switch Design with Self Aligning and Sub-Lithographic Properties**

BETR Faculty: Tsu-Jae King Liu

*Tech ID: 18962*

**Improved Mechanical Contact Reliability and Energy Efficiency for CMOS Applications**

BETR Faculty: Tsu-Jae King Liu

*Tech ID: 18103*

**Nanowire-based Chemical Connector for Miniature-Scale Applications**

BETR Faculty: Ali Javey

*Tech ID: 17830*

**Low Cost, Low-Temperature Polycrystalline Semiconductor Films for Solar Cells and Large Scale Integrated Circuits**

BETR Faculty: Tsu-Jae King Liu

*Tech ID: 17658*

**Ultra-low-power and Robust Integrated Circuits for Logic and Memory**

BETR Faculty: Tsu-Jae King Liu

*Tech ID: 17370*

**Low Voltage Mems Flash Memory**

BETR Faculty: Tsu-Jae King Liu

*Tech ID: 17319*

**Platform for Batch Integration of Dissociated or Incompatible Technologies**

BETR Faculty: Tsu-Jae King Liu

*Tech ID: 17172*

**Improved DRAM With Capacitorless Double-gate**

BETR Faculty: Tsu-Jae King Liu

# 4 Appendices

*BETR Solid State Technology and Devices Seminar*

*May 7, 2021*

# Innovations for Continuation of Moore's Law During Next 10 Years

Tahir Ghani
Intel Senior Fellow
Director, Process Pathfinding Program
Intel Corporation

**Abstract:** Integrated circuit technologies have had a profound impact on the human society during the last 50 years. An early pioneer of integrated circuit age, Gordon Moore projected in 1965 that the transistor density would double every year, which he later modified to doubling every 2 years. An exponential increase in the transistor density during the last 5-decades has continued unabated. As a consequence, the transistor density for the state-of-the-art logic technology is now ~1-2M transistors/mm$^2$. The enormity of the challenges in maintaining an exponential growth over a period of 5-decades has led many naysayers to periodically announce the impending demise of Moore's Law. However, despite the enormity, these challenges have been surmounted, thanks to the ingenuity of generations of research and development engineers. With the critical dimensions now scaling to sub-10nm regime, there is again an increasing concern that the transistor density has reached close to a plateau. However, I believe that these concerns are again misplaced. In my talk I plan to present new innovations which will enable transistor density to continue to grow during foreseeable future (~10 years). I will describe Gate-all-Around transistor and subsequently a Vertically-Stacked transistor structure, which will serve as the foundation for improving the density and performance/watt metric in future. An increasing role of on-die interconnects, patterning innovations using EUV and novel packaging technologies will serve as effective solutions to improve density and performance at reasonable cost. Finally, I will highlight the ever increasing role of Design-Technology-Co-Optimization (DTCO) towards achieving density and performance improvement beyond pitch reduction. A combination of new transistors, novel interconnects and packaging, EUV patterning, and next generation DTCO tools is expected to enable continuation of Moore's Law into the future, with density reaching ~1B transistors/mm$^2$.

**Bio:** Dr. Tahir Ghani is a Senior Fellow and Director of Process Pathfinding Program at Intel Corporation. He received his PhD in Electrical Engineering from Stanford University in 1994. Since joining Intel in 1994, he has led the teams responsible for developing some of the most significant changes in semiconductor industry and implementing them into mainstream CMOS manufacturing. These include uniaxial strained silicon transistors, HiK+Metal Gate transistors and FinFET transistors. He currently leads Intel's Pathfinding Program with focus on technology definition, evaluation of new process innovations and demonstrating their early viability for technologies beyond 2025. His contributions have been recognized by many awards including IEEE Jun-ichi Nishizawa Medal in 2012. He is a Fellow of the IEEE and was elected to the U.S. National Academy of Engineering in 2015.

*BETR Solid State Technology and Devices Seminar*

*May 14, 2021*

# Magnonic Spintronics: Toward Spin Wave Based Information Processing

Luqiao Liu
Associate Professor
Department of Electrical Engineering and Computer Science
MIT

**Abstract:** Spin wave is considered as one of the promising candidates for realizing unconventional computing and interconnection. Compared with other forms of waves, spin wave has many unique features, including short wavelength, intrinsic nonlinearity, non-reciprocity, etc. In this talk I will discuss some of our recent efforts in studying transport properties of spin wave (or equivalently, magnons) in various magnetic structures. In the first example, I will show that there exist mutual interactions between magnons and magnetic domain walls in a ferromagnet, where domain walls change the phase and magnitude of spin waves, and a strong spin wave in turn moves the position of domain walls. This mutual interaction can be used to realize a programmable spin wave phase shifter. In the second example, I will talk about long-range spin transport in an easy-plane antiferromagnet, where the spin angular momentum propagates via the superposition of two linearly polarized magnon modes. We show that the magnon transport in this antiferromagnet can be used to build a non-volatile spin current switch. These mechanisms and device structures could be used as building blocks for future magnon based information processing in the classical and quantum domain.

**Bio:** Dr. Luqiao Liu is an Associate Professor of Electrical Engineering at Massachusetts Institute of Technology. He received his B.S. in physics from Peking University in 2006, and Ph.D. in Applied Physics from Cornell University in 2012. He worked as a Research Staff Member at IBM Watson Research Center before joining MIT in 2015. Luqiao's current research focuses on spintronic material and devices for memory, logic and communication applications. Luqiao Liu has received the award of McMillan Award, NSF Career Award, Air Force Young Investigator Award, Sloan Fellowship, and International Union of Pure and Applied Physics Young Scientist Award.

*BETR Solid State Technology and Devices Seminar*

*September 17, 2021*

# Electronics and Spintronics in 2D Materials

Sanjay K. Banerjee
Cockrell Chair Professor of Electrical and Computer Engineering
Microelectronics Research Center
University of Texas at Austin

**Abstract:** 2D materials such as graphene and transition metal dichalcogenides have opened up avenues in mechanically flexible circuits for IoT applications, and low power, beyond-CMOS device concepts. We will discuss processing challenges such as growth and doping of these materials. We will also discuss our work involving 2D-2D tunneling in these materials, leading to transistors with negative differential resistance. Other 2D materials such as topological insulators and transition metal oxides have applications in spintronics. They can be used for beyond-CMOS, non-volatile low power logic and memory devices.

**Bio:** Dr. Sanjay Banerjee is the Cockrell Chair Professor of Electrical and Computer Engineering and Director, Microelectronics Research Center, at the University of Texas at Austin. He has over 1000 archival refereed publications/talks, 10 books/chapters, and 35 U.S. patents. He has received the SIA/SRC University Researcher Award (2017), IEEE Grove Award (2014), ECS Callinan Award (2003), and is a Fellow of IEEE, APS and AAAS. He is active in beyond-CMOS logic and memory devices, and fabrication and modeling of advanced MOSFETs.

*Solid State Technology and Devices Seminar*

*October 1, 2021*

# High Power Diffraction-Limited Tapered Diode Lasers

Dr. Jenna Campbell
Director of High Power Laser Engineering
Freedom Photonics

**Abstract:** Broad area diode lasers operate with high power and efficiency but suffer from poor beam quality. These devices are incoherent, multimode sources that cannot be focused effectively on a distant target. Nearly diffraction-limited output is critical for applications including directed energy, wireless power beaming, and automotive LIDAR. These applications are presently dominated by diode-pumped laser architectures which rely on the use of “brightness converters”; in this configuration, the light from diode lasers is used to pump another laser medium with high quality single mode output, such as rare earth doped solid-state crystals or glass fibers. These brightness converters add cost and complexity and sacrifice efficiency, wasting 50% or more of the injected diode laser energy by turning it into heat. Recent advancements in diffraction-limited output from tapered diode lasers represent a disruptive technology breakthrough that is poised to revolutionize the laser industry by eliminating the need for the brightness converter. We have demonstrated a new world record of >3 W nearly diffraction-limited output power from a 1550 nm InP edge-emitting tapered diode laser. These devices are operated in continuous wave (CW) mode at room temperature. Our GaAs tapered lasers deliver >9 W output power at 885 nm and 980 nm. These results are enabled by a novel structured contact which permits geometric scaling of the chip dimensions while preserving beam quality.

**Bio:** Dr. Jenna Campbell is the Director of High Power Laser Engineering at Freedom Photonics, a small business in Santa Barbara, California that specializes in the design and manufacturing of high performance semiconductor lasers and photonic components. Over the past few years, her team has been developing world-class high power lasers, including single mode diode lasers, tapered amplifiers and lasers, and high power fiber-coupled modules. Prior to joining Freedom Photonics, she completed her PhD in Physics at the University of California Santa Barbara, where her experimental research focused on photon—spin interactions of embedded quantum dots in photonic crystal microcavities. Dr. Campbell is an active member of the photonics community and has authored or co-authored >40 conference papers and peer-reviewed articles.

*BETR Solid State Technology and Devices Seminar*

*October 15, 2021*

# Towards Optical Quantum Networks Based on Rare-Earth Ions and Nano-Photonics

Andrei Faraon
Professor of Applied Physics and Electrical Engineering
California Institute of Technology

**Abstract:** Optical quantum networks for distributing entanglement between quantum machines will enable distributed quantum computing, secure communications and new sensing methods. These networks will contain quantum transducers for connecting computing qubits to travelling optical photon qubits, and quantum repeater links for distributing entanglement at long distances. In this talk I discuss implementations of quantum hardware for repeaters and transducers using rare-earth ions, like ytterbium and erbium, exhibiting highly coherent optical and spin transitions in a solid-state environment. We show that single ytterbium ions in nano-photonic resonators are well suited for optically addressable quantum bits with long spin coherence, single shot readout, good optical stability, and local access to nuclear spin wave quantum memory registers. These single qubits will form the backbone of future quantum repeater networks and will be augmented by optical storage and linear processing capabilities, also implemented using rare-earth ions. Towards this end we demonstrated optical quantum storage using erbium ensembles coupled to silicon photonics, where the frequency and release time of the stored photon can be controlled using on-chip electronics. Finally, to connect the optical network to superconducting quantum computers, we develop optical to microwave quantum transducers based on rare-earth ensembles simultaneously coupled to on-chip optical and microwave superconducting resonators. I conclude by addressing the remaining challenges for interconnecting these components into future quantum networks.

**Bio:** Dr. Andrei Faraon is a Professor of Applied Physics and Electrical Engineering at California Institute of Technology. After earning a B.S. degree in physics with honors in 2004 at California Institute of Technology, he received his M.S. in Electrical Engineering and PhD in Applied Physics both from Stanford University in 2009. From 2009 to 2012 he was a postdoctoral fellow at Hewlett Packard Laboratories. During his PhD he was involved in seminal quantum optics experiments using single semiconductor quantum dots coupled to photonic crystal resonators. At HP, he pioneered quantum nano-photonic devices in single crystal diamond coupled to color centers. Dr. Faraon left HP in 2012 for a faculty position at Caltech where he works on nano-photonic technologies for both classical and quantum applications including: optically addressable quantum bits, optical quantum memories, microwave to optical quantum transduction, metasurfaces and metamaterials for multi-functional imaging applications. Dr. Faraon is the recipient of the 2018 Adolph Lomb Medal of the Optical Society of America (OSA) that recognizes a noteworthy contribution to optics made by a researcher who is still early in his or her career and was elected as OSA Fellow in 2020. He was also awarded the 2015 National Science Foundation CAREER award, the 2015 Air Force Office of Scientific Research young investigator award and the 2016 Office of Naval Research Young Investigator Award.

*BETR Solid State Technology and Devices Seminar*

*October 22, 2021*

# Quanta Image Sensor (QIS), or, Detecting Single Electrons in Silicon at Room Temperature, Without Avalanche Multiplication, in a Commercial Product

Eric R. Fossum
John H. Krehbiel Sr. Professor for Emerging Technologies
Dartmouth Engineering, Thayer School
Dartmouth College

**Abstract:** The Quanta Image Sensor (QIS) was conceived as a different image sensor – one that counts photoelectrons one at a time using perhaps a billion, small, specialized pixels, read out at high frame rate, perhaps thousands of frames per second. A gray-scale image (or color image) is created post-capture from the collected data using computation imaging or machine-learning approaches. Over the past 6 or so years, pixels that can count a single electron or resolve electron number directly at room temperature, without avalanche multiplication, have been invented and demonstrated at Dartmouth. A 1-Mpixel QIS device was implemented in the TSMC 65nm/45nm stacked backside-illuminated CMOS image sensor process and demonstrated to function. Soon thereafter, Gigajot Technology Inc was spun off from Dartmouth to further commercialize QIS devices. In this talk, the device concept, device implementation(s), and results will be presented. Recent progress at Dartmouth on improving the devices will be introduced. Product data from Gigajot, that uses the technology developed for QIS for deep-sub-electron read noise, will be also be included, time permitting.

**Bio:** Dr. Eric R. Fossum is best known for the invention of the CMOS image sensor "camera-on-a-chip" used in billions of cameras. He is a solid-state image sensor device physicist and engineer, and his career has included academic and government research, and entrepreneurial leadership. He is the John H. Krehbiel Sr. Professor for Emerging Technologies at the Dartmouth Engineering, directs the Dartmouth's Ph.D. Innovation Programs and serves as Dartmouth's Vice Provost for Entrepreneurship and Technology Transfer. In 2017, Dr. Fossum received the Queen Elizabeth Prize from HRH Prince Charles, considered by many as the Nobel Prize of Engineering "for the creation of digital imaging sensors," along with three others. He was inducted into the National Inventors Hall of Fame and elected to the National Academy of Engineering. Other honors include the 2020 OSA and IS&T Edwin Land Medal, the IEEE Andrew Grove Medal, the SMPTE Camera Origination and Imaging Medal, and Yale's Wilbur Cross Medal. He is also the first and only Dartmouth Engineering professor to win an Emmy Award. Dr. Fossum has published over 300 technical papers and holds over 175 US patents. He co-founded several startups and served as CEO. He also co-founded the International Image Sensor Society (IISS) and was its first President. He is a Fellow member of the Institute of Electrical and Electronic Engineers (IEEE) and the Optical Society of America (OSA).

*Solid State Technology and Devices Seminar*

*October 29, 2021*

# Transient Electronics

John A. Rogers
Louis Simpson and Kimberly Querrey Professor of Materials Science and Engineering
McCormick School of Engineering
Northwestern University

**Abstract:** A remarkable feature of modern integrated circuit technology is its ability to operate in a stable fashion, with almost perfect reliability, without physical or chemical change. Recently developed classes of electronic materials create an opportunity to engineer the opposite outcome, in the form of 'transient' devices that dissolve, disintegrate, degrade or otherwise disappear at triggered times or with controlled rates. Water-soluble classes of transient electronic devices serve as the foundations for applications in zero-impact environmental monitors, 'green' consumer electronic gadgetry and bio-resorbable biomedical implants. This presentation describes the foundational concepts in materials science, electrical engineering and assembly processes for building bio/ecoresorbable electronics in a variety of formats and with a range of functions. Wireless sensors of intracranial temperature, pressure and electrophysiology designed for monitoring recovery from a traumatic brain injury, stimulators configured for accelerating neuroregeneration of an injured peripheral nerve and temporary pacemakers for minimizing risks after a cardiac surgery provide some system level examples.

**Bio:** Professor John A. Rogers obtained BA and BS degrees in chemistry and in physics from the University of Texas, Austin, in 1989. From MIT, he received SM degrees in physics and in chemistry in 1992 and the PhD degree in physical chemistry in 1995. From 1995 to 1997, Rogers was a Junior Fellow in the Harvard University Society of Fellows. He joined Bell Laboratories as a Member of Technical Staff in the Condensed Matter Physics Research Department in 1997, and served as Director of this department from the end of 2000 to 2002. He then spent thirteen years on the faculty at University of Illinois, most recently as the Swanlund Chair Professor and Director of the Seitz Materials Research Laboratory. In the Fall of 2016, he joined Northwestern University as the Louis Simpson and Kimberly Querrey Professor of Materials Science and Engineering, Biomedical Engineering and Medicine, with affiliate appointments in Mechanical Engineering, Electrical and Computer Engineering and Chemistry, where he is also Director of the recently endowed Querrey Simpson Institute for Bioelectronics. He has published more than 700 papers, is a co-inventor on more than 100 patents and he has co-founded several successful technology companies. His research has been recognized by many awards, including a MacArthur Fellowship (2009), the Lemelson-MIT Prize (2011), the Smithsonian Award for American Ingenuity in the Physical Sciences (2013), the MRS Medal (2018) and most recently the Benjamin Franklin Medal from the Franklin Institute (2019). He is a member of the National Academy of Engineering, the National Academy of Sciences, the National Academy of Medicine, the National Academy of Inventors and the American Academy of Arts and Sciences.

*BETR Solid State Technology and Devices Seminar*

*November 5, 2021*

# Color Center in Silicon: From Ensembles to Single Qubit

Walid Redjem
Postdoctoral Researcher, Kante Group
Electrical Engineering and Computer Science
UC Berkeley

**Abstract:** Given its potential for integration and scalability, silicon is likely to be a key platform for large-scale quantum technologies. Individual electron-encoded artificial atoms, formed by either impurities or quantum dots, have emerged as a promising solution for silicon-based integrated quantum circuits. However, single qubits featuring an optical interface, which is needed for long-distance exchange of information, have never been studied for quantum technologies applications. During this seminar I will first introduce recent photoluminescence measurements from an ensemble of color centers in heavily carbon implanted commercial silicon. Especially I will address the recombination dynamics of a G-center in silicon involving a three-level system. In the second part I will report for the first time the isolation of single optically active point defects from low fluence carbon implanted silicon. These artificial atoms exhibit a bright, linearly polarized single-photon emission with a quantum efficiency of the order of unity. This single-photon emission occurs at telecom wavelengths suitable for long-distance propagation in optical fibers. Our results show that silicon can accommodate single isolated optical point defects like in wide-bandgap semiconductors, despite a small bandgap (1.1 eV) that is unfavorable for such observations.

**Bio:** Dr. Walid Redjem completed his master's degree in quantum devices at University of Paris Diderot in 2016, before joining University of Montpellier in France as a Ph.D. Student. There he worked mainly of color center in silicon for quantum technologies applications. And showed for the first time, the possibility of isolating single silicon color center. In 2020 he joined Boubacar Kante's group at UC Berkeley – EECS, as a post-doc where is developing new types of classical and quantum light sources based on topological photonics.

*BETR Solid State Technology and Devices Seminar*

*November 8, 2021*

# Advanced Packaging, Heterogeneous Integration, and the Future of Semiconductor Systems

Prof. Madhavan Swaminathan
John Pippin Chair in Microsystems Packaging & Electromagnetics
School of Electrical and Computer Engineering
Georgia Tech

**Abstract:** The semiconductor industry is headed towards heterogeneous integration in 2.5D or 3D form being driven by the high cost of monolithic integration, time to market and the need for extreme heterogeneity. This is great news for packaging. At Georgia Tech we have been developing a platform technology called System on Package (SOP) for many years. One embodiment of this technology, which represents a recent breakthrough, is a non-TSV (through silicon via) based 2.5D/3D integration using fanout panel level glass packaging that provides unprecedented opportunities for emerging applications such as wireless and high-performance computing. This presentation will discuss the rationale for such an approach, recent results, ongoing research, and its comparison with fanout wafer level packaging pursued by industry today.

**Bio:** Madhavan Swaminathan is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE), Professor in ECE with a joint appointment in the School of Materials Science and Engineering (MSE), and Director of the 3D Systems Packaging Research Center (PRC), Georgia Tech (GT) (http://www.prc.gatech.edu). He also serves as the Site Director for the NSF Center for Advanced Electronics through Machine Learning (CAEML: https://publish.illinois.edu/advancedelectronics/) and Leads the Heterogeneous Integration area, at the SRC JUMP ASCENT Center (https://ascent.nd.edu/). Prior to joining GT, he was with IBM working on packaging for supercomputers. He is the author of 530+ refereed technical publications and holds 31 patents. He is the primary author and co-editor of 3 books and 5 book chapters, founder and co-founder of two start-up companies (JMD and E-System Design), and founder of the IEEE Conference on Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the IEEE Electronics Packaging Society (EPS). He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE Electromagnetic Compatibility (EMC) society. He received his MS and PhD degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.

*BETR Solid State Technology and Devices Seminar*

*November 12, 2021*

# High Performance Graphene Nanoribbon Transistors

Zafer Mutlu
Postdoctoral Researcher, Bokor Group
Electrical Engineering and Computer Science
UC Berkeley

**Abstract:** Recent advances in on-surface organic synthesis have led to the development of rational bottom-up graphene nanoribbon (GNR) growth with atomic precision.[1] This atomic precision leads to versatile electronic properties tailored by the widths and edge topologies, which make GNRs promising candidates for future transistor technologies and quantum information processing.[2] However, a range of fundamental synthesis, integration, and materials science challenges have impeded the fabrication of devices with the expected performance.[3] Here, recent progress in integrating bottom-up synthesized GNRs into devices will be presented. [4-6] GNR transistors with high on-state current and excellent switching performance were successfully fabricated. The transistor structures fabricated include back-gate and double-gate field-effect transistors (FETs). Challenges and opportunities of GNRs as transistor channels will be discussed, together with possible further improvements and potential future research directions.

[1] J. Cai et al, Atomically Precise Bottom-up Fabrication of Graphene Nanoribbons, *Nature* 2010, 466, 470.
[2] H. Wang et al., Graphene Nanoribbons for Quantum Electronics, *Nature Reviews Physics*, 2021.
[3] V. Saraswat et al., Materials Science Challenges to Graphene Nanoribbon Electronics, *ACS Nano* 2021, 15, 3674.
[4] Z. Mutlu et al., Transfer-Free Synthesis of Atomically Precise Graphene Nanoribbons on Insulating Substrates, *ACS Nano* 2021, 15, 2635.
[5] Z. Mutlu et al., Bottom-Up Synthesized Nanoporous Graphene Transistors, *Advanced Functional Materials*, 2021 (in press).
[6] Z. Mutlu et al., Short-Channel Double-Gate FETs with Atomically Precise Graphene Nanoribbons*, IEDM* 2021 (accepted).

**Bio:** Dr. Zafer Mutlu is a postdoctoral researcher with Prof. Jeffrey Bokor in the Department of Electrical Engineering and Computer Sciences (EECS) at University of California, Berkeley and a research affiliate at the Molecular Foundry at Lawrence Berkeley National Laboratory (LBNL). He is also part of the Berkeley Emerging Technologies Research (BETR) Center. He received his PhD in Materials Science and Engineering from University of California, Riverside in 2016, where he continued his postdoctoral research until joining to Berkeley in 2018. His current research focuses on bottom-up synthesis and nanoelectronics devices of graphene nanoribbons. His doctoral research was on the synthesis and phase engineering of two-dimensional materials. His research work has appeared in highly respected journals, including ACS Nano, Nano Energy, JACS, and Advanced Functional Materials, and in top conferences, including IEEE International Electron Devices Meeting (IEDM), Semiconductor Research Corporation (SRC) TECHCON Conference, American Physical Society (APS) Meeting, Materials Research Society (MRS) Meeting, and the International Society for Optics and Photonics (SPIE) Meeting.

*BETR Solid State Technology and Devices Seminar*

*November 19, 2021*

# Microscopic Robots

Paul McEuen
John A. Newman Professor of Physical Science
Director, Kavli Institute at Cornell for Nanoscale Science
Cornell University

**Abstract:** Can we build microscopic robots? Autonomous ambulatory creatures too small to be resolved by the naked eye? The brains are not the problem: a modern IC has tens of thousands of transistors in the area occupied by a paramecium. But two major components are missing: electronic actuators that can operate as the robot's micro-appendages, and a power/communication system for getting energy/info in and out. In this talk, I will discuss work by an interdisciplinary team at Cornell to create tiny robots. We first created OWiCs, or Optical Wireless Integrated Circuits, that use light for comms and power. OWiCs are smartphones for the micro world, with potential applications in everything from implantable sensors to microscopic ID tags, or here, for the brains of a microscopic robot. For appendages, we developed a new class of electrochemical actuators called SEAs that readily flex on the micron scale. We then integrated SEAs with OWiCs to build our first prototype microscopic robots, which now hold a Guinness World Record for the Smallest Walking Robot. But what are they good for? To quote Benjamin Franklin: "What good is newborn baby?"

**Bio:** Dr. Paul McEuen is the John A. Newman Professor of Physical Science at Cornell University and Director of the Kavli Institute at Cornell for Nanoscale Science. His research explores the electronic, optical, and mechanical properties of nanoscale materials; he is currently excited about using these materials to construct functional, intelligent micron-scale sensors and robots. He is also a novelist, and his scientific thriller SPIRAL (featuring tiny robots) won the debut novel of the year from the International Thriller Writers Association. He is a fellow of the American Physical Society, the National Academy of Sciences, and the American Academy of Arts and Sciences. He is also a co-founder of OWiC Technologies, an early-stage startup commercializing the Optical Wireless Integrated Circuit platform.

*BETR Solid State Technology and Devices Seminar*

*December 10, 2021*

# Critical Demand and Supply Trends in Semiconductors

Rutger Vrijen
Partner
McKinsey & Company

**Abstract:** Current semiconductor shortages are a significant source of economic pain for Original Equipment Manufacturers (OEM's), with the largest crunch being felt by the Automotive industry. Although the Covid pandemic was an important trigger for these shortages, structural strain in the semiconductor supply chain had been building prior to it. In response to the shortages, semiconductor buyers as well as national governments are re-evaluating their views on the strategic importance of semiconductor sourcing. At the same time, major manufacturers (foundries and integrated device manufacturers) are announcing record-breaking capital investment plans to build new capacity. This presentation will review several critical trends driving semiconductor demand and supply, and implications for the global semiconductor supply chain.

*Or, the short version for students: Semiconductors are hot again! You're in the right field!*

**Bio:** Dr. Rutger Vrijen is a Partner in McKinsey's global Semiconductor and Advanced Electronics practice. He serves semiconductor and other advanced-electronics clients on a range of topics, including growth strategy and transformation, cross-border M&A, pricing excellence for channel and direct sales, supply-chain performance diagnostics and transformation, as well as effective, efficient product development. Prior, Rutger was at NXP Semiconductors, where he was Senior VP and Head of Strategy for Business Unit Security & Connectivity (~$4B annual revenues), and general Manager of the RFID Tagging business. In this role, he oversaw the integration of Freescale Semiconductor ($40B merger). Early in his career Rutger was a Staff Engineer at Sun Microsystems, where he led prototype development projects on UltraSparc III processor performance and reliability. Rutger holds two patents and has published over 30 articles in globally leading scientific journals. He has a Ph.D. in Physics from the University of Amsterdam, performed post-doctoral research in Electrical Engineering at UCLA, and he has an MBA from Erasmus University Rotterdam.

*BETR Solid State Technology and Devices Seminar*

Friday, February 18, 2022

# Convergence of Electronics and Photonics in CMOS Integrated Systems for Classical and Quantum Optical Interconnects, Sensing and Scalable Integrated Photonic Apertures

Miloš Popović

Associate Professor
Electrical and Computer Engineering
BU Photonics Center
Boston University

**Abstract:** The monolithic integration of electronics and photonics – and advanced CMOS platforms supporting it – have evolved over the past decade from a futuristic area of research to the state of the art for photonic systems-on-chip. I will start by briefly overviewing my and collaborators' work on advanced CMOS platforms, initial landmark demonstrations and commercial spinoff, and both the subsequent foundry development and new applications that has fueled. We started with limited photonic device performance, where the overall system provided a win, but today have record performance in a number of photonic components. The convergence of electronics and photonics has driven both foundry process developments trading and advancing photonics vs. electronics, and has called for foundry-process aware innovations in device design. In this talk, I will talk about two recent efforts as illustrations, and provide examples of other projects. In the first part of my talk, I will describe the development of a highly robust integrated beam splitter, a basic component of complex photonic circuits. I will share with you a new electromagnetic concept, rapid adiabatic mode evolution, and its use to develop an integrated beam splitter of unsurpassed bandwidth, insertion loss, splitting ratio, and robustness against process uncertainty. The approach is a fundamental step beyond current state of the art adiabatic devices, the gold standard for insensitive design over the past 30 years. I'll also show an experimental demonstration of record performance (loss, split ratio), including wafer scale variation data, in a state of the art, soon to be public state CMOS photonics platform (GlobalFoundries 45CLO). I'll provide an overview of other high performance components, and share some examples of applications currently being pursued in quantum and cryogenic I/O. In the second part of my talk, I will talk about scalable integrated photonic apertures for lidar, imaging, sensing and spectrometry. Even with complex integrated systems approaching reality, the complexity circuits needed for large area integrated optical apertures using conventional integrated optical phased arrays is excessive and doesn't scale well with area. I will talk about a new concept involving a tiled-array aperture and computationally-aided imaging to get around the inherent sensitivities of integrated photonics. The building block is the serpentine optical phased array (SOPA), a nominally passive tile allowing 2D wavelength steering. I will show the concept, experimental demonstrations, and initial demonstrations of Fourier basis imaging which allows imaging without beam forming, i.e. allows beam forming in post processing. I'll also describe application

of the SOPA to spectrometers, where the device has resolving power comparable to bulk grating spectrometers far outperforming integrated ones, with a footprint comparable to integrated spectrometers, far smaller than bulk. SOPAs may find utility not only in lidar but also spaceborne instruments and mobile devices.

**Bio:** Dr. Miloš Popović is an Associate Professor of Electrical and Computer Engineering at Boston University, and a Principal Investigator in the BU Photonics Center where he leads a research group in the area of integrated photonics. He is also a Co-Founder and Technical Advisor of Ayar Labs. Miloš earned his B.Sc. in Electrical Engineering from Queen's University, Canada in 1999, and his PhD from MIT in 2007. His interests are in the conception, theory, simulation and design of novel integrated photonic devices and systems, and in the monolithic integration of CMOS electronics and photonics in platforms allowing "vertically integrated", fast innovation from the device level through system and application. He is an author or co-author of over 40 patents and 240 journal and conference papers, and is a 2012 Fellow of the Packard Foundation.

*BETR Solid State Technology and Devices Seminar*

Friday, March 4, 2022

# Diffractive Optical Networks & Computational Imaging Without a Computer


Aydogan Ozcan

Chancellor's Professor and the Volgenau Chair for Engineering Innovation
Electrical and Computer Engineering & Bioengineering
California NanoSystems Institute
University of California, Los Angeles



**Abstract:** We will discuss diffractive optical networks designed by deep learning to all-optically implement various complex functions as the input light diffracts through spatially-engineered surfaces. These diffractive processors complete their computational task at the speed of light propagation through thin, passive optical layers and will find various applications in e.g., all-optical image analysis, feature detection, object classification, computational imaging and sensing, also enabling task-specific camera designs and new optical components.


**Bio:** Dr. Ozcan is the Chancellor's Professor and the Volgenau Chair for Engineering Innovation at UCLA and an HHMI Professor with the Howard Hughes Medical Institute, leading the Bio- and Nano-Photonics Laboratory at UCLA and is also the Associate Director of the California NanoSystems Institute. Dr. Ozcan is elected Fellow of the National Academy of Inventors (NAI), holds more than 50 issued/granted patents and >20 pending patent applications, and is the author of one book and the co-author of >700 peer-reviewed publications in major scientific journals and conferences. Dr. Ozcan is the founder and a member of the Board of Directors of Lucendi Inc., Pictor Labs, Hana Diagnostics and Holomic/Cellmic LLC, which was named a Technology Pioneer by The World Economic Forum in 2015. Dr. Ozcan is also a Fellow of the American Association for the Advancement of Science (AAAS), the International Photonics Society (SPIE), the Optical Society of America (OSA), the American Institute for Medical and Biological Engineering (AIMBE), the Institute of Electrical and Electronics Engineers (IEEE), the Royal Society of Chemistry (RSC), the American Physical Society (APS) and the Guggenheim Foundation, and has received major awards including the Presidential Early Career Award for Scientists and Engineers, International Commission for Optics Prize, Biophotonics Technology Innovator Award, Rahmi M. Koc Science Medal, International Photonics Society Early Career Achievement Award, Army Young Investigator Award, NSF CAREER Award, NIH Director's New Innovator Award, Navy Young Investigator Award, IEEE Photonics Society Young Investigator Award and Distinguished Lecturer Award, National Geographic Emerging Explorer Award, National Academy of Engineering The Grainger Foundation Frontiers of Engineering Award and MIT's TR35 Award for his seminal contributions to computational imaging, sensing and diagnostics. Dr. Ozcan is also listed as a Highly Cited Researcher by Web of Science, Clarivate.

*BETR Solid State Technology and Devices Seminar*

Friday, March 11, 2022

# Advanced Logic Technology: Trends and Challenges

Dr. Victor Moroz

Synopsys Fellow
Editor, IEEE Electron Device Letters
Synopsys Inc.

**Abstract:** Lithographic feature scaling pace started to slow down at 10nm node and is expected to stop scaling after 2nm node. Despite that, we see Moore's law continuing at least for the next 10 years with annualized transistor density increase of ~20% and annualized reduction of cost per transistor of ~15%. This progress is enabled by increasingly sophisticated DTCO (Design-Technology Co-Optimization). This work illustrates DTCO applied to advanced CMOS logic and SRAM to explore and quantify different innovations in design and technology. One illustration is about the role of transistor variability as the driving force behind industry transitions from planar MOSFET to FinFET to GAA technologies. Another illustration highlights evolution of stress engineering for planar MOSFETs, FinFETs, and GAA technologies. Yet another key topic that we will cover is the self-heating and heat escape engineering challenges.

**Bio:** Dr. Victor Moroz received M.S. degree in Electrical Engineering from Novosibirsk Technical University in Siberia and Ph.D. degree in Applied Physics from the University of Nizhny Novgorod. After engaging in technology development at several semiconductor manufacturing companies and teaching semiconductor physics at the University, Dr. Moroz joined a Stanford spin-off Technology Modeling Associates in 1995. After IPO in 1997, the TMA TCAD team became part of Avanti in 1998, and in 2002 it became a key part of Synopsys, connecting a synthesis company to the manufacturing. Currently Dr. Moroz is a Synopsys Fellow, engaged in a variety of projects on modeling advanced CMOS with over 300 granted and pending US and international patents, and serving as an Editor of IEEE Electron Device Letters.

*BETR Solid State Technology and Devices Seminar*

Friday, March 18, 2022

# Multimode Fiber Optics and Applications

Hui Cao

John C. Malone Professor of Applied Physics
Department of Applied Physics
Yale University

**Abstract:** Multimode optical fibers have broad applications in communication, imaging, sensing and high-power lasers. However, random mode coupling and polarization mixing cause severe spatial and temporal distortions of optical signals. By adjusting the spatial profile of an incident field, we achieve a full control of the temporal shape and polarization state of light transmitted through a multimode fiber. Furthermore, a multimode fiber can function as a high-resolution, low-loss spectrometer. We utilize the speckle patterns from a multimode fiber to achieve single-shot full-field recovery of ultrashort optical pulses.

**Bio:** Dr. Hui Cao is the John C. Malone Professor of Applied Physics, a Professor of Physics, and a Professor of Electrical Engineering at Yale University. She received her Ph.D. degree in Applied Physics from Stanford University. Prior to joining the Yale faculty, she was on the faculty of Northwestern University. Her technical interests and activities are in the areas of mesoscopic physics, complex photonic materials and devices, nanophotonics, and biophotonics. Cao authored or co-authored one monograph, twelve book-chapters, seven review articles and 260 journal papers. She is a member of the National Academy of Sciences, and the American Academy of Arts and Sciences.

BETR Solid State Technology and Devices Seminar

Friday, April 8, 2022

High-Throughput Single-Molecule Assays Using DNA Origami

Ashwin Gopinath
Assistant Professor
Department of Mechanical Engineering
MIT

Abstract: Single-molecule bioassays have enabled us to significantly improve our understanding of biological systems by unmasking underlying heterogeneity, in molecular systems, that is often hidden in ensemble experiments. These assays typically involve the collection of highly noisy data and processed insights being directly correlated to the throughput of the experiments. Thus, the challenges associated with the controllable manipulation and organization of individual molecules, present a significant challenge to the development of high-throughput single-molecule devices. In this talk, I will introduce a directed self-assembly technique to organize arbitrary molecules on planar substrates, using DNA origami, as well as its use in creating novel single-molecule devices and high-throughput bioassays. Finally, I will describe a generalized method for templating inorganic materials onto DNA origami while maintaining all the key programmability of DNA origami to further increase the throughput of experiments dealing with single-molecule manipulation.

Bio: Dr. Ashwin Gopinath is an Assistant Professor in the Department of Mechanical Engineering at MIT. His research is at the intersection of self-assembly, micro-fabrication, biophysics and machine learning. Dr. Gopinath obtained his Ph.D. in from Boston University, was as a research scientist at Caltech and Google before starting his independent group at MIT in 2019. He has co-authored 21 papers in journals like Nature, Science and PNAS as well as received several awards, most recent of which is the Robert Dirk Prize in Molecular Programming for his seminal contributions in merging DNA nanotechnology with conventional semiconductor nanofabrication.

*BETR Solid State Technology and Devices Seminar*

Friday, April 15, 2022

# Minimally Invasive Neural Interfaces: Battery-free Bioelectronics and Lensless Microscopes

Jacob T. Robinson

Associate Professor
Electrical and Computer Engineering & Bioengineering
Rice University

**Abstract:** Miniature implanted devices capable of manipulating and recording biological signals promise to improve the way we study biology and the way we diagnose and treat disease; however, to create technologies that are both small and effective we must overcome myriad engineering challenges. In this talk, I will describe two efforts to create these minimally invasive bioelectronics. In the first case I will describe flat, lensless microscopes that can image brain activity in mice and non-human primates [1]. In the second case, I will describe miniature, battery-free bioelectronic technologies that receive data and power via magnetoelectric materials. These materials offer a platform for safe and reliable power delivery for networks of miniature bioelectronic implants capable of distributed closed-loop therapies [2,3]. Overall, these approaches for minimally invasive bioelectronics could support next-generation brain-computer interfaces and more effective bioelectronic medicine.

1. Adams, J.K., Yan, D., Wu, J. et al. In vivo lensless microscopy via a phase mask generating diffraction patterns with high-contrast contours. Nat. Biomed. Eng. (2022). https://doi.org/10.1038/s41551-022-00851-z
2. Singer, A., Dutta, S., Lewis, E. et al. Magnetoelectric Materials for Miniature, Wireless Neural Stimulation at Therapeutic Frequencies, Neuron (2020). https://doi.org/10.1016/j.neuron.2020.05.019
3. Chen, J.C., Kan, P., Yu, Z. et al. A wireless millimetric magnetoelectric implant for the endovascular stimulation of peripheral nerves. Nat. Biomed. Eng. (2022). https://doi.org/10.1038/s41551-022-00873-7

**Bio:** Dr. Jacob Robinson received a B.S. in Physics from UCLA in 2003 and a Ph.D. in Applied Physics from Cornell University in 2008 under advisor Dr. Michal Lipson. After completing his Ph.D., studying silicon nanophotonics, he began postdoctoral research in the Department of Chemistry and Chemical Biology at Harvard University. While at Harvard, Jacob developed silicon nanowire devices to probe the electrical and chemical activity of living cells. In the summer of 2012, he joined the ECE and BioE departments at Rice. He is currently interested in developing nanofabricated devices to study the structural and functional dynamics of living neural circuits.

*BETR Solid State Technology and Devices Seminar*

Friday, April 22, 2022

# Innovation in Semiconductors for High Voltage

Dr. Ahmad Bahai

Senior Vice President and Chief Technology Officer
Texas Instruments

**Bio:** Dr. Ahmad Bahai, is a senior vice president and chief technology officer (CTO) of Texas Instruments responsible for guiding break-through innovation, corporate research and Kilby Labs. Dr. Bahai is an Adjunct professor at Stanford University, and IEEE Fellow. He was a professor in residence at UC Berkeley from 2001-2010. Throughout his career, Dr. Bahai has held a number of leadership roles including director of research labs and chief technology officer of National Semiconductor, technical manager of a research group at Bell Laboratories and founder of Algorex, a communication and acoustic IC and system company, which was acquired by National Semiconductor. He holds a Master of Science in Electrical Engineering from Imperial College, University of London and a doctorate degree in Electrical Engineering from University of California, Berkeley.

*BETR Solid State Technology and Devices Seminar*

Friday, April 29, 2022

# Understanding Radiative Recombination in Two Dimensional Semiconductors

Shiekh Zia Uddin
Graduate Student, Javey Group
Electrical Engineering and Computer Science
UC Berkeley

**Abstract:** Two-dimensional (2D) materials have shown exceptional promise in various electronic and optoelectronic applications with prospects of improved performance compared to traditional technologies. Some unique advantages include the ability to create van der Waals (vdW) heterostructures, many-body physics, and various approaches to band structure engineering. Unlike the free-carrier characteristics of conventional semiconductors, the photophysics of 2D materials is governed by excitons, which are the primary format of photogenerated carriers at room temperature due to their strong binding energies. In this talk I will show that because of this excitonic nature the carrier recombination can be entirely radiative in monolayer transition metal dichalcogenides, as long as the photogenerated carriers are in the form of neutral excitons. As a result, the photoluminescence (PL) quantum yield (QY), defined as the ratio of photons emitted to photons absorbed, can approach unity at all generation rates even in the presence of a high native defect density. I will then talk about the excitonic to free-carrier transition in black phosphorus and show that the PL QY is highest at the monolayer limit when it is excitonic. This uniquely robust tolerance to defects presents a key advantage of 2D semiconductors over conventional semiconductors toward developing highly efficient optoelectronics, as stringent growth and fabrication requirements for high-quality crystals can be lowered.

**Bio:** Shiekh Zia Uddin is a Ph.D. candidate in Prof. Ali Javey's group. His research is focused on carrier recombination in low-dimensional semiconductors. He received his Bachelors in Science degree in Electrical and Electronics Engineering from Bangladesh University of Engineering and Technology (BUET), where he worked on both biomedical signal processing and nanophotonics.

*BETR Solid State Technology and Devices Seminar*

Friday, May 6, 2022

# Micro-Electro-Mechanical Relay Technology for Beyond Von Neumann Architecture

Xiaoer Hu
Graduate Student, Liu Group
Electrical Engineering and Computer Science
UC Berkeley

**Abstract:** Micro-electro-mechanical (MEM) relays previously have been shown to be promising for energy-efficient digital computing applications, due to their abrupt ON/OFF switching characteristics and negligible off-state leakage current. In this talk, novel applications of MEM relays will be presented. First, we will demonstrate that MEM relays can operate reliably with millivolt signals at cryogenic temperatures, due to much lower hysteresis voltage and more stable ON-state resistance. A sub-10 mV relay-based inverter circuit is demonstrated at a temperature of 4 K. Our experimental study indicates that MEM relays should be able to operate at temperatures as low as 1.8 K, making them promising candidates for ultra-low power cryogenic digital interface circuits for quantum computing. Second, the DC-bias-dependent oscillatory behavior of MEM relays is investigated via experimental study and finite-element-method-based computer simulations. Sub-harmonic injection locking and coupled oscillation behaviors of MEM relays are demonstrated, indicating that MEM relay oscillators are promising for implementing Ising machines, which can solve combinatorial optimization problems much more efficiently than conventional computer architectures.

**Bio:** Xiaoer Hu is a Ph.D. candidate in Professor Tsu-Jae King Liu's group. Her research is focused on novel applications of micro-electro-mechanical relays. She received her bachelor's degree in Materials Science and Engineering from the University of Michigan, Ann Arbor in 2017, and a bachelor's degree in Electrical and Computer Engineering from Shanghai Jiao Tong University in 2017.

# Spring 2021 Workshop *Online*

betr
Berkeley Emerging Technologies Research Center

**May 27-28, 2021**

**UC Berkeley Zoom Platform**

**Thursday, May 27**

| | | |
|---|---|---|
| ***12:00 PM*** | ***Closed Session:***<br>***Current BETR Corporate Affiliates and BETR co-Directors*** | |
| | - *Opening Remarks* | *Tsu-Jae King Liu* |
| | - *Center Management Updates* | *Michael Bartl* |
| | - *Corporate Affiliates' Dialog with the BETR Center* | *Jeffrey Bokor (Moderator)* |
| **1:00 PM** | **Open Session: Welcome** | |
| **1:05 PM** | **BETR Research Presentations** | |
| 1:05 PM | "Electric Field Control of Magnetism for Beyond CMOS Electronics" | Ramamoorthy Ramesh |
| 1:30 PM | "Towards Monolithically Integrated Hybrid CMOS-NEM Circuits" | Urmita Sikder (Liu group) |
| 1:55 PM | "Towards Ultimately Scaled Transistors with Low-Dimensional Materials" | Yuxuan Cosmi Lin (Bokor group) |
| *2:20 PM* | *Break* | |
| **2:40 PM** | **Preview of New BETR Website** | Michael Bartl, Haochen Gao |
| **2:55 PM** | **BETR Research Presentations** | |
| 2:55 PM | "Onsager Computing versus Quantum Computing" | Eli Yablonovitch |
| 3:20 PM | "Ising Computing: Compositional Training and Parallel Asynchronous Sampling" | Sayeef Salahuddin |
| *3:45 PM* | *Break* | |
| **4:00 PM** | **Current Trends, Opportunities and Challenges in the Semiconductor Industry**<br>***Industry Panel Discussion***<br>*with Questions from BETR Students and Postdocs* | Moderators: Urmita Sikder and Lars Tatum |
| **5:00 PM** | **Day 1 Wrap-Up** | |

# Spring 2021 Workshop *Online*

betr
Berkeley Emerging Technologies Research Center

**May 27-28, 2021**

**UC Berkeley Zoom Platform**

**Friday, May 28**

| | | |
|---|---|---|
| **8:00 AM** | **Open Session: Welcome** | |
| **8:10 AM** | **Student & Postdoc Lightning Talks** | |
| | "Actively Tunable Midwave/Longwave IR Emitters and Detectors" | Hyungjin Kim (Javey group) |
| | "Fully Integrated Electronic-Photonic Biosensor for Label-Free Molecular Sensing in Advanced Zero-Change CMOS-SOI Process" | Christos Adamopoulos (Stojanovic group) |
| | "Printed Miniaturized Li-ion Batteries for Autonomous Microsystems" | Anju Toor (Arias group) |
| | "Printed Biodegradable IDE Capacitor for Humidity Monitoring" | Emma Wawrzynek (Arias group) |
| | "Picometer Phase Metrology for EUV Masks" | Stuart Sherwin (Waller group) |
| | "Naturally Degradable Nitrate Sensors for Precision Agriculture" | Payton Goodrich (Arias group) |
| | "Generation of Picosecond Current Pulse with Auston Switch on Arbitrary Substrate Using Layer Transfer Technique" | Hanuman Singh (Bokor group) |
| | "Self-Oscillation of MEM Relays" | Xiaoer Hu/Lars Tatum (Liu group) |
| | "Hybrid Reservoir Computing for Image Recognition" | Philip Jacobson (Wu group) |
| | "Antiferromagnetic Switching in NiO/Pt Bilayers with Large Domains" | Sucheta Mondal (Bokor group) |
| | "Novel spin-orbit torque generation at room temperature in an all-oxide epitaxial $La_{0.7}Sr_{0.3}MnO_3/SrIrO_3$ system" | Xiaoxi Huang (Ramesh group) |
| | "Monolithically Integrated Electronic-Photonic Ultrasound Receiver Array" | Panagiotis Sarkos (Stojanovic group) |
| | "EUV microscope characterization using photomask surface roughness" | Gautam Gunjala (Waller group) |
| *9:10 AM* | *Break* | |
| **9:30 AM** | **BETR co-Director Presentations** | |
| 9:30 AM | "Printed Flexible Sensors" | Ana Arias |
| 9:55 AM | "Computational Imaging for Metrology" | Laura Waller |
| *10:20 AM* | *Break and Switch to Zoom Breakout Rooms* | |
| **10:30 AM** | **Student & Postdoc Virtual Poster Session** *(Zoom Breakout Rooms)* | |
| ***11:30 AM*** | ***Closed Session: Feedback – BETR Corporate Affiliates and BETR co-Directors*** | |
| **12:00 PM** | **Adjournment** | |

# Fall 2021 Workshop *Online*

betr
Berkeley Emerging Technologies Research Center

**November 15-16, 2021**

*All times are Pacific time*

**Monday, November 15:** *Zoom link: https://berkeley.zoom.us/j/94689993616*

| | | |
|---|---|---|
| ***12:00 PM*** | ***Closed Session: Current BETR Corporate Affiliates and BETR co-Directors*** | |
| | - *Opening Remarks* | *Tsu-Jae King Liu* |
| | - *Center Management Updates* | *Michael Bartl* |
| | - *Corporate Affiliates' Dialog with the BETR Center* | *Jeffrey Bokor (Moderator)* |
| **1:00 PM** | **Open Session: Welcome** | |
| **1:10 PM** | **BETR Research Presentations** | |
| 1:10 PM | "Next-Generation Deep-Learning Accelerators: From Hardware to System" | Sophia Shao |
| 1:30 PM | "Study of DC-Driven MEM Relay Oscillators for Implementation of Ising Machines" | Xiaoer Hu |
| 1:50 PM | "Machine Acceleration of Many-Body Quantum Mechanics" | Pratik Brahma |
| *2:10 PM* | *Break* | |
| **2:30 PM** | **Special Session: Workforce Development** | |
| 2:30 PM | "American Semiconductor Academy" | Tsu-Jae King Liu |
| 2:45 PM | Open Discussion | |
| *3:30 PM* | *Break* | |
| **3:50 PM** | **BETR Research Presentations** | |
| 3:50 PM | "Graphene Nanoribbon Transistors" | Jeffrey Bokor |
| 4:10 PM | "Flexible Blade-coated Devices: Dual Functionality with Simultaneous Deposition" | Jasmine Jan |
| 4:30 PM | "Printed, Li-ion Miniature Batteries for On-chip Electronics" | Anju Toor |
| **4:50 PM** | **Day 1 Wrap-Up** | |

# Fall 2021 Workshop *Online*

betr
Berkeley Emerging Technologies Research Center

**November 15-16, 2021**

*All times are Pacific time*

**Tuesday, November 16:** *Zoom link:* https://berkeley.zoom.us/j/95236679451

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|---|---|---|
| **8:00 AM** | **Open Session: Welcome** | |
| **8:05 AM** | **BETR Research Presentations** | |
| 8:05 AM | "Reconfigurable Silicon Photonic Integrated Circuits" | Ming Wu |
| 8:25 AM | "Bright Emission Across the Spectrum with a Generic Electroluminescent Device" | Vivian Wang |
| 8:45 AM | "Improvements in Modeling, Design, and Metrology for EUV Photomasks" | Stuart Sherwin |
| 9:05 AM | "Electronic-Photonic Systems on Chip" | Vladimir Stojanović |
| *9:20 AM* | *Break* | |
| **9:35 AM** | **Student & Postdoc Lightning Talks** | |
| | "Nonvolatile Electric Field Control of Inversion Symmetry" | Lucas Caretta (Ramesh group) |
| | "Electric Field Control of Thermal Magnons in BiFeO3" | Eric Parsonnet (Ramesh group) |
| | "Spin-Orbit Torque Rectifier for Weak RF Energy Harvesting" | Shehrin Sayeed (Salahuddin group) |
| | "Double-Gate Graphene Nanoribbon FETs" | Zafer Mutlu (Bokor group) |
| | "MOSFET Exhibiting Negative Differential Resistance (NDR-FET) for Embedded Memory Applications" | Lars Tatum (Liu group) |
| | "Workload Characterization of Ray Tracing" | Hansung Kim (Shao group) |
| | "A Co-Simulation Platform Enabling the Performance Characterization of Quadrotor SoCs" | Dima Nikiforov (Shao group) |
| | "Characterization and Comparison of Biodegradable Printed Capacitive Humidity Sensors" | Emma Wawrzynek (Arias group) |
| | "Naturally Degradable Nitrate Sensors for Precision Agriculture" | Payton Goodrich (Arias group) |
| | "Low-Loss Wafer-Bonded Silicon Photonic MEMS Switches" | Amirmahdi Honardoost (Wu group) |
| | "Electronic-Photonic Cryogenic Egress Link" | Bozhi Yin (Stojanović group) |
| | "CMOS Quantum Photonics" | Daniel Kramnik (Stojanović group) |
| | "EUV Microscope Characterization Using Photomask Surface Roughness" | Gautam Gunjala (Waller group) |
| *10:25 AM* | *Break and Switch to Zoom Breakout Rooms* | |
| **10:30 AM** | **Student & Postdoc Virtual Poster Session** (Zoom Breakout Rooms) | |
| ***11:30 AM*** | ***Closed Session: Feedback – BETR Corporate Affiliates and BETR co-Directors*** | |
| **12:00 PM** | **Adjournment** | |