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Berkeley Emerging Technologies Research Center

Annual Report

May 2022 – April 2023

Questions regarding this report or requests for additional information should be directed to:

Michael H. Bartl
Executive Director
Berkeley Emerging Technologies Research (BETR) Center
University of California, Berkeley
Office: 510-664-7814
Mobile: 213-400-5895
Email: mbartl@berkeley.edu

Table of Contents (with clickable direct-links)

The Berkeley Emerging Technologies Research Center

1.1 Executive Statement

Established in 2016, the Berkeley Emerging Technologies Research (BETR) Center is a hub of physical electronics research at the University of California, Berkeley. It serves as a nexus for interactions between faculty and student researchers and leading technology companies for long-term research collaborations. The goal of the BETR Center is to be a knowledge exchange by providing the central infrastructure needed to bring together diverse groups of researchers and decision makers from the semiconductor industry and academia. Research activities in the BETR Center thus span a wide range from the search for new materials and manufacturing processes to the development of novel computing and memory devices and the design of heterogeneous integrated systems.

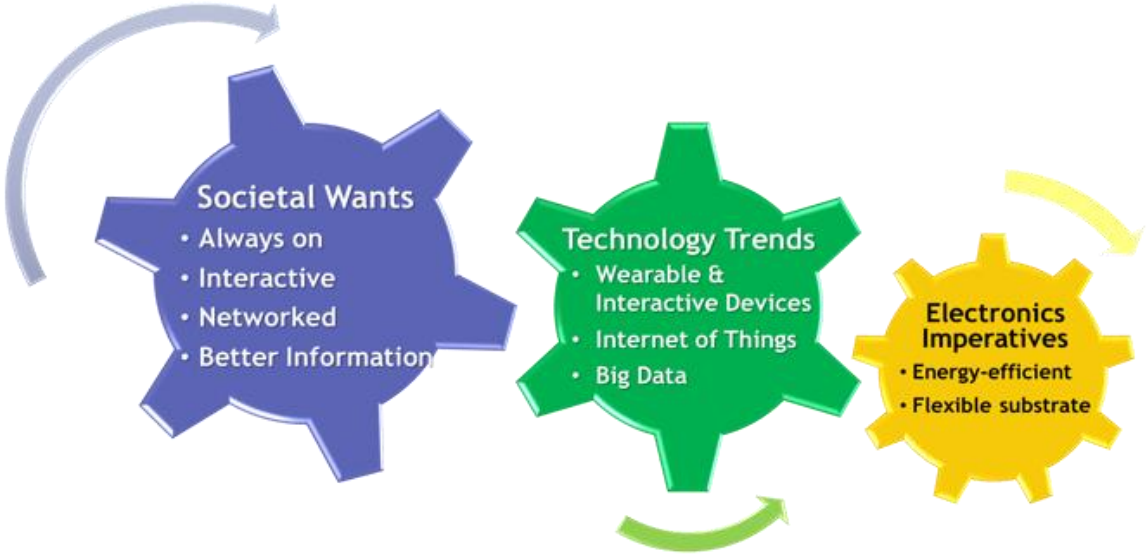
The mission of the BETR Center is to foster innovation in materials, processes, and devices toward the vision of ubiquitous information systems for enhancing health and quality of life in our global society.

For the last five decades, steady miniaturization of the transistor has yielded continual improvements in integrated-circuit performance and cost per function, with dramatic impact on virtually every aspect of life in modern society. This proliferation of information and communication technologies has enabled cloud computing and the Internet of Things, which

together with recent advancements in artificial intelligence and machine learning give rise to the vision of a fully *interconnected world* with systems for coordinating critical infrastructure for *smart cities*, managing personalized health care and medicine for *smart hospitals*, automating vehicles and traffic flow for *smart highways*, and optimizing manufacturing and logistics for *smart factories*.

The real-time processing of large quantities of data required by artificially intelligent systems is possible today because of the dramatic improvement of the capabilities of computing devices. This exponential increase of computation power in the last 120 years is described in Kurzweil's Law, which predicts that computing systems are rapidly approaching the capability of the human brain. Underlying Kurzweil's Law is Moore's Law, describing the evolution of transistors fueled by advancements in materials, processes, and structures that have enabled transistors to be miniaturized to sub-20 nm feature sizes in the most advanced chips today. However, as fundamental limits are approached, transistor scaling will not be as straightforward in the future as it has been in the past. Alternative approaches for improving chip functionality, cost per function and energy efficiency eventually will thus be necessary to sustain the rapid growth of the semiconductor industry beyond the next decade.

The BETR Center is ideally positioned to address these challenges by bringing together a broad range of world-renowned leaders in electronic devices and technology research. The BETR team of UC Berkeley professors, postdocs, and students collaborates across the disciplines of electrical engineering, computer science and materials science to build the technological foundation for future ubiquitous information systems. Considering that artificially intelligent systems must always be awake, interactive, and networked across many devices, it is imperative that future electronic systems are more energy efficient to be ubiquitous, and they need to be compatible with flexible substrates to be wearable.



1.2 Leadership Team

To meet the need for a new industry growth paradigm (beyond Moore's Law), the BETR Center brings together research leaders whose collective expertise spans materials, structures, and manufacturing processes for nanoelectronics, nanomagnetics, optoelectronics, metrology, and IC design and system architecture. In fact, BETR faculty co-directors have contributed significant innovations to sustain Moore's Law in the last few decades, including the development of "spacer lithography" (self-aligned double patterning, SADP) for patterning of sub-lithographic features, the "FinFET" (a fin-shaped field-effect transistor structure) for transistor scaling to below 10 nm, and most recently the "negative capacitance FET" to reduce transistor operating voltage.

Faculty co-Directors *(in alphabetical order)*

Ana Claudia Arias

Dr. Ana Claudia Arias is a professor in the Department of Electrical Engineering and Computer Science at UC Berkeley. She received her Ph.D. in Physics from the University of Cambridge, UK in 2001. Prior to that, she received her master's and bachelor's degrees in physics from the Federal University of Paraná in Curitiba, Brazil in 1997 and 1995, respectively.

Dr. Arias joined the University of California, Berkeley in January of 2011. Before that she was manager of the Printed Electronic Devices Area and a Member of Research Staff at PARC, a Xerox Company. She went to PARC, in 2003, from Plastic Logic in Cambridge, UK where she led the semiconductor group. Her research focuses on the use of electronic materials processed from solution in flexible electronic systems. Dr. Arias uses printing techniques to fabricate flexible large area electronic devices and sensors.

Jeffrey Bokor

Dr. Jeffrey Bokor is the Paul R. Gray Distinguished Professor of Engineering in the Department of Electrical Engineering and Computer Sciences at UC Berkeley, with a joint appointment as Senior Scientist in the Materials Science Division at Lawrence Berkeley National Laboratory.

Dr. Bokor received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology in 1975, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1976 and 1980, respectively. From 1980 to 1993, he was at AT&T Bell Laboratories where he did research on a variety of topics in laser science, advanced lithography for integrated circuits, as well as semiconductor physics and technology, and held several management positions.

Dr. Bokor joined the Berkeley faculty in 1993 and served in a number of administrative positions including Associate Dean for Research in the College of Engineering, and Chair of the Electrical Engineering and Computer Science Department. His current research activities include nanomagnetics/spintronics, graphene electronics, nanophotonics, and nano-electromechanical systems. He is a fellow of IEEE, APS, and OSA.

Ali Javey

Dr. Ali Javey is the Lam Research Distinguished Chair in Semiconductor Processing and a professor of Electrical Engineering and Computer Sciences at UC Berkeley. He is a co-director of Berkeley Sensor and Actuator Center (BSAC), and also a senior faculty scientist at the Lawrence Berkeley National Lab where he serves as the program leader of Electronic Materials (E-Mat).

Dr. Javey received a Ph.D. degree in chemistry from Stanford University in 2005 and was a Junior Fellow of the Harvard Society of Fellows from 2005 to 2006 before joining the faculty at UC Berkeley. His research interests encompass the fields of chemistry, materials science, and electrical engineering and focus on the integration of nanoscale electronic materials for various technological applications, including low power electronics, flexible circuits and sensors, and energy generation and harvesting.

Dr. Javey is the recipient of numerous awards, including the Dan Maydan Prize in Nanoscience Research, the MRS Outstanding Young Investigator Award, the Nano Letters Young Investigator Lectureship, the National Academy of Sciences Award for Initiatives in Research, Technology Review TR35, and the NSF Early CAREER Award.

Tsu-Jae King Liu

Dr. Tsu-Jae King Liu is the Dean of the College of Engineering and the Roy W. Carlson Professor of Engineering at UC Berkeley. Previously, she served as Chair of the EECS Department, the COE Associate Dean for Research, and Faculty Director of the Marvell Nanolab. She was also Sr. Director of Engineering in the Advanced Technology Group of Synopsys, Inc. (2004-06).

She received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from Stanford University. She joined the Xerox Palo Alto Research Center as a Member of Research Staff in 1992, to research and develop high-performance thin-film transistor technologies for flat-panel display applications. In 1996 she joined the faculty at UC Berkeley. Her research activities are presently in advanced materials, fabrication processes and devices for energy-efficient electronics. She has authored or co-authored over 550 publications and holds over 95 patents.

Dr. Liu's awards include the DARPA Significant Technical Achievement Award for development of the FinFET, the IEEE Kiyo Tomiyasu Award, the Intel Outstanding Researcher in Nanotechnology Award, and the Semiconductor Research Corporation (SRC) Aristotle Award. Dr. Liu is a fellow of the IEEE, a member of the U.S. National Academy of Engineering, and a fellow of the National Academy of Inventors. She serves on the Board of Directors for Intel Corporation and on the Board of Directors for MaxLinear, Inc.

Sayeef Salahuddin

Dr. Sayeef Salahuddin is the TSMC Distinguished Professor of Electrical Engineering and Computer Sciences at UC Berkeley. He is the co-director of the Berkeley Center for Negative Capacitance Transistors (BCNCT) and Berkeley Device Modeling Center (BDMC), and an associate director of ASCENT, a multi-university center within the DARPA/SRC JUMP initiative.

His group explores physics for low power electronic and spintronic devices. He is mostly known for the discovery of the Negative Capacitance effect that shows substantial promise for logic, memory and energy storage devices.

Dr. Salahuddin Salahuddin received the Presidential Early Career Award for Scientist and Engineers (PECASE) from President Obama. Salahuddin also received several other awards including the National Science Foundation CAREER award, the IEEE Nanotechnology Early Career Award, the Young Investigator Awards from the Airforce Office of Scientific Research and the Army Research Office, and the IEEE George E Smith Award. He served on the editorial board of IEEE Electron Devices Letters (2013-16) and was the chair the IEEE Electron Devices Society committee on Nanotechnology (2014-16). Salahuddin currently serves as the Editor-in-Chief of the IEEE Electron Devices Letters. Salahuddin is a Fellow of the IEEE and the APS.

Sophia Shao

Dr. Sophia Shao is an Assistant Professor and an SK Hynix Faculty Fellow in Electrical Engineering and Computer Sciences at UC Berkeley. Previously, she was a Senior Research Scientist at NVIDIA Research.

Dr. Shao received her Ph.D. degree in 2016 and S.M. degree in 2014 from Harvard University. Her research interests are in the area of computer architecture, with a special focus on specialized accelerator, heterogeneous architecture, and agile VLSI design methodology.

Dr. Shao's work has been awarded the Best Paper Award at DAC 2021, the Best Paper Award at JSSC 2020, a Best Paper Award at MICRO 2019, Top Picks in Computer Architecture (2014), and Honorable Mentions (2019*2). Her Ph.D. dissertation was nominated by Harvard for ACM Doctoral Dissertation Award. Dr. Shao is an SK Hynix Faculty Fellow and the recipient of an NSF

CAREER Award, the 2022 IEEE TCCA Young Computer Architect Award, a Google Faculty Rising Stars Award in Systems Research, a Facebook Research Award, an Okawa Foundation Research Grant, and the inaugural Dr. Sudhakar Yalamanchili Award.

Vladimir Stojanović

Dr. Vladimir Stojanović is Professor of Electrical Engineering and Computer Science at UC Berkeley. He received his Ph.D. in Electrical Engineering from Stanford University in 2005, and the Dipl. Ing. degree from the University of Belgrade, Serbia in 1998. He was also with Rambus, Inc., Los Altos, CA, from 2001 through 2004 and with MIT as Associate Professor from 2005 to 2013.

Research interests of Dr. Stojanović include design, modeling and optimization of integrated systems, from CMOS-based VLSI blocks and interfaces to system design with emerging devices like NEM relays and silicon-photonics. He is also interested in design and implementation of energy-efficient electrical and optical networks, and digital communication techniques in high-speed interfaces and high-speed mixed-signal IC design.

Dr. Stojanović received the IBM Faculty Partnership Award, the NSF CAREER Award, the ICCAD William J. McCalla, the IEEE Transactions on Advanced Packaging, and the ISSCC Jack Raper best paper award. He was an IEEE Solid-State Circuits Society Distinguished Lecturer for the 2012-2013 term.

Laura Waller

Dr. Laura Waller is the Charles A. Desoer Professor of Electrical Engineering and Computer Sciences at UC Berkeley, leading the Computational Imaging Lab. She also has affiliations in Bioengineering and Applied Sciences & Technology. From 2016 to 2020 Dr. Waller held the UC Berkeley Ted Van Duzer Endowed Professorship.

Dr. Waller was a Postdoctoral Researcher and Lecturer of Physics at Princeton University from 2010-2012 and received B.S., M.Eng. and Ph.D. degrees from Massachusetts Institute of Technology in 2004, 2005 and 2010, respectively. She is a Moore Foundation Data-Driven Investigator, Bakar fellow, Distinguished Graduate Student Mentoring awardee, NSF CAREER awardee, Chan-Zuckerberg Biohub Investigator, SPIE Early Career Achievement Awardee, Optica Adolph Lomb Medal recipient, and a Packard Fellow.

Ming C. Wu

Dr. Ming C. Wu is Nortel Distinguished Professor of Electrical Engineering and Computer Sciences and Co-Director of the Berkeley Sensor and Actuator Center (BSAC) at UC Berkeley. Dr. Wu received his B.S. degree in Electrical Engineering from National Taiwan University in 1983, and M.S. and Ph.D. degrees in Electrical Engineering and Computer Sciences from UC Berkeley in 1986 and 1988, respectively. He was Member of Technical Staff at AT&T Bell Laboratories, Murray Hill (1988-1992) and Professor of Electrical Engineering at the University of California, Los Angeles (1992-2004). He has been a faculty member at Berkeley since 2004.

His research interests include silicon photonics, optoelectronics, MEMS, MOEMS, and optofluidics. He has published 8 book chapters, over 600 papers in journals and conferences, holds 30 U.S. patents. His research has been successfully commercialized by OMM (MEMS optical switches, 1997) and Berkeley Lights (NASDAQ:BLI, optofluidics, 2011).

Prof. Wu is Fellow of IEEE and Optical Society (OSA), and was a Packard Foundation Fellow (1992-1997). He was a member of the IEEE Photonics Society Board of Governors (2013-2016). His work has been recognized by the 2016 IEEE Photonics Society William Streifer Scientific Achievement Award, the 2007 Paul F. Forman Engineering Excellence Award, the 2017 C.E.K. Mees Medal from the Optical Society (OSA), and the 2020 Robert Bosch Micro and Nano Electro Mechanical Systems Award from IEEE Electron Device Society.

Eli Yablonovitch

Dr. Eli Yablonovitch is the James & Katherine Lau Chair Emeritus in Engineering in the Department of Electrical Engineering and Computer Sciences, and Professor in the Graduate School at UC Berkeley. He is also the Director Emeritus of the NSF Center for Energy Efficient Electronics Science (E3S), a National Science Foundation funded multi-University Center headquartered at Berkeley. Dr. Yablonovitch received his Ph.D. degree in Applied Physics from Harvard University in 1972. He worked for two years at Bell Telephone Laboratories, and then became a professor of Applied Physics at Harvard. He joined Exxon in 1979 and Bell Communications Research in 1984, before joining UCLA in 1992. Since 2007 he is a faculty member at UC Berkeley.

Prof. Yablonovitch introduced the idea that strained semiconductor lasers could have superior performance due to reduced valence band (hole) effective mass. With almost every human interaction with the internet, optical telecommunication occurs by strained semiconductor lasers. He is regarded as a Father of the Photonic BandGap concept, and he coined the term “Photonic Crystal”. The geometrical structure of the first experimentally realized Photonic bandgap, is sometimes called “Yablonovite”. In his photovoltaic research, Prof. Yablonovitch introduced the 4(n squared) (“Yablonovitch Limit”) light-trapping factor that is in worldwide use, for almost all commercial solar panels. His mantra that “a great solar cell also needs to be a great LED”, is the

basis of the world record solar cells: single-junction 29.1% efficiency; dual-junction 31.5%; quadruple-junction 38.8% efficiency; all at 1 sun.

Dr. Yablonovitch is elected as a Member of the National Academy of Engineering, the National Academy of Sciences, the National Academy of Inventors, the American Academy of Arts & Sciences, and is a Foreign Member of the Royal Society of London. Among his many awards are the OSA Ives-Quinn Medal, the Benjamin Franklin Medal, the IEEE Edison Medal, the Isaac Newton Medal, the Buckley Prize, the IEEE W.R. Cherry Award, and the Adolf Lomb Medal.

Executive Director

Michael H. Bartl

Dr. Michael H. Bartl is the executive director of the Berkeley Emerging Technology Research (BETR) Center. He also serves as deputy director of the MUSE Energy Frontier Research Center at the University of Utah, where he is a research professor. As the BETR Center executive director, he oversees all center activities, provides leadership and strategic direction, leads the coordination of research efforts, and manages center staff.

Before moving to Berkeley, Dr. Bartl was a tenured professor in chemistry at the University of Utah, and a visiting professor at the Technical University of Munich, Germany. He co-founded Navillum Nanotechnologies, a start-up company focused on fabrication of nanostructured semiconductors. Dr. Bartl served as deputy editor for Scripta Materialia and authored more than 70 publications about his research activities in functional nanostructured materials for energy and information technology applications.

Dr. Bartl earned his doctorate degree in materials/inorganic chemistry from Karl-Franzens University Graz, Austria, before conducting postdoctoral research at the University of California, Santa Barbara. He was the recipient of a “DuPont Young Professorship” and was named a “Brilliant 10” researcher by Popular Science magazine and a Scialog Fellow by the Research Corporation for Science Advancement.

1.3 Corporate Membership

The BETR Center was established with the goal to foster long-term academia-industry research collaborations and knowledge transfer by connecting UC Berkeley faculty and students who are building the technological foundation for future electronic devices and information systems with leading semiconductor companies. The BETR Center model of mutually beneficial collaborations gives corporate members early access to innovative ideas and research results, while university researchers gain insights into technological challenges faced by industry and society, and by seeing the results of their research applied to solve real-world problems. Moreover, the BETR Center provides various opportunities for member companies to interact directly with its faculty co-directors and 100+ graduate students and postdocs, many of whom are prospective future employees.

Since its inception in 2016, the BETR Center has seen a steady increase in the number of corporate members, and we are delighted to currently have eight leading companies in innovation in the semiconductor industry be part of the BETR Center. These companies are (in alphabetical order): AMD, Applied Materials, Atomera, Intel Corporation, Lam Research, Meta (formerly Facebook), SK Hynix, and TSMC.

Each of the member companies is represented in the BETR Center Technical Advisory Board (TAB). The TAB meets biannually as part of the BETR Center Workshops in a closed session to promote dialog between industry and academia. As such, the TAB is a crucial body in providing all BETR faculty co-directors important feedback for on-going research and future directions. Moreover, since the TAB comprises members from across the industrial ecosystem, it provides

BETR Center researchers with multiple and holistic perspectives. Additional benefits of a BETR Center corporate membership include:

Access to Periodic Research Webinars

During the fall and spring semesters, the BETR Center hosts a series of webinars featuring leading-edge research within the fields of physical electronics and optoelectronics. Given by researchers from UC Berkeley and other research institutions, these webinars are accessible via an online meeting service. Recordings of most of these webinars are made available to corporate members via password-protected access on the BETR website. In the 2022/23 reporting period, the BETR Center hosted and shared 20 webinars (see Appendix A for details).

Attendance at Semi-Annual Research Reviews/Workshops

The BETR Center holds two research reviews/workshops per year in which the latest research results are presented. These events include oral presentations, industry panels, and lightning talks and poster sessions by BETR students and postdocs, offering an opportunity to meet and interact with student presenters, who are potential candidates for internships and/or employment. In 2022, two BETR Workshops were held (agendas for the spring in-person and online events are given as Appendix B and Appendix C, respectively, and the agenda for the fall event is attached as Appendix D).

Invitation to Berkeley EECS Annual Research Symposium (BEARS)

Each year in February, UC Berkeley's Department of Electrical Engineering and Computer Sciences hosts a day-long research conference featuring a variety of informative talks by distinguished faculty members and advanced graduate students. BEARS gives industrial affiliates a look at some of the most exciting research being pursued in information science and technology.

Customized Briefings

Upon request, the BETR Center staff will facilitate the scheduling of meetings with individual BETR Center co-directors. Based on best efforts, they will also facilitate introductions to other research centers and programs at UC Berkeley, as well as to companies that are part of UC Berkeley's technology innovation ecosystem.

Option to Direct Part of the Membership Contribution to a Faculty co-Director

Each corporate affiliate may direct part of the monetary membership contribution to specific research project(s) or research team(s). Typically, this is request is made at the start of the annual membership period. The BETR Center co-directors will then review requests and endeavor to allocate part of the contribution to support those research topics. Acknowledgment of the company's support will be made in all publication of the results from studies that are funded specifically by the allocated portion of the company's gift.

Facilitation of Technology Licensing

Twice a year, a list of research publications and patent applications will be provided to all industry affiliates. Upon request, the BETR Center staff will facilitate introductions to the Industry Alliances Office and Office of Technology Licensing at UC Berkeley for technology licensing.

2 Research Activities

2.1 Motivation and Overview

The central goal of the BETR Center is to provide solutions for driving innovation in materials, processes and solid-state devices to enable future ubiquitous information systems. Research activities are motivated by three main challenges for *ambient intelligence* to become a reality:

Looming Power Crisis for Computing: Electricity consumed by computing devices has increased exponentially with the proliferation of information and communication technology. To avoid a power crisis in the future, fundamentally new concepts for more energy-efficient logic switches and on-chip communication are needed. In addition to breakthroughs in solid-state science and technology, innovations in circuit design and system architecture will be necessary to avert a power crisis for computing.

Advent of the Internet of Things: The Internet of Things era of ubiquitous computing, wherein electronic devices are pervasive and wirelessly networked with access to cloud computing requires heterogeneous integration to diversify functionality and mechanical flexibility in mobile devices. For these to be affordable, new manufacturing techniques must be developed through interdisciplinary research into novel tools, processes, and materials that are compatible with low-cost plastic substrates.

Proliferation of Big Data Applications: "Big Data" has become the main driver for advances in memory technology and high-performance computing with increasing need for storing and processing large data sets in real-time to derive actionable information. Hardware innovations (including non-von-Neumann architectures) and new computational algorithms and software systems will be needed to meet the demand within reasonable energy and cost constraints.

Finding solutions to these grand challenges requires a concerted effort across disciplines and between academic and industrial researchers. In response, the BETR Center assembled a diverse group of UC Berkeley professors from electrical engineering, computer science and materials science, working with industry researchers, to build the technological foundation for future electronic devices and information systems. The BETR Center research teams are organized in six distinct, but highly collaborative, research thrusts (Figure 1): (1) Next-Generation Devices (including Millivolt Switches and Embedded Memory), (2) Flexible Electronics, (3) Accelerators for AI, (4) System Integration, (5) Optical Interconnects, (6) Metrology. In the following, information for each of the research thrusts is provided, including key achievements in the last twelve months and a description of current and future projects.

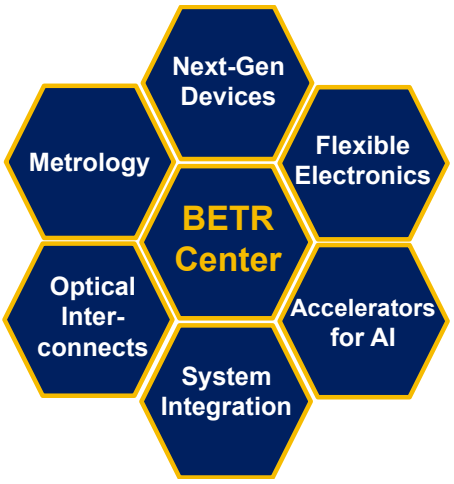


Figure 1. Research Thrusts of the BETR Center.

2.2 Thrust 1: Next-Generation Devices

*Research activities of the Next-Generation Devices Thrust have been supported in part by directed membership contributions of **TSMC**, **SK Hynix**, **Intel Corporation**, and **Atomera**.*

Recent advancements in cloud computing, social networking, mobile internet and data analytics, and the associated increase of battery-powered electronic systems, will require the development of new intelligent systems with custom properties. In particular, the transition from traditional computing to mobile approaches necessitate logic switches and memory systems that can operate at significantly reduced power consumption and higher speeds. Central to the BETR Center's research mission is thus the development of next-generation energy-efficient electronic devices and integrated systems. In fact, many of the ultra-low power electronics research projects in the BETR Center have originated in the Center for Energy Efficient Electronics Science (E^3S) based on the recognition that the energy used to manipulate a single bit of information is currently ~100,000 times greater than the theoretical limit. Research on next-generation devices and circuits in the BETR Center is conducted by **Professors Jeffrey Bokor**, **Ali Javey**, **Tsu-Jae King Liu**, **Sayeef Salahuddin**, **Vladimir Stojanović**, and **Eli Yablonovitch**, and encompasses the search for new materials and device architectures as alternatives to classical transistor-based digital logic and memory. Examples include new circuit and system architectures leveraging zero-leakage nano-electromechanical (NEM) relays, field effect transistors (FETs) with 2D materials as active layers, graphene nanoribbon transistors, and ultrafast magnetic switches.[NG1-NG4]

2.2.1 Recent Achievements

A. Graphene Nanoribbons

In the last view years, the BETR team, led by the **Bokor** group (with BETR associated faculty researcher, Prof. Felix Fischer) has successfully synthesized several distinct graphene nanoribbons (GNRs) with ultra-narrow width (0.7-3.0 nm) and developed processes to integrate GNRs into functioning FETs. While individual devices displayed excellent switching behavior with ON/OFF ratios of ~10^5 and ON-currents (I_{ON}) of ~60 nA,[NG4,NG5] performance variations are still poorly understood but need to be overcome for widespread use of GNR-based technology.

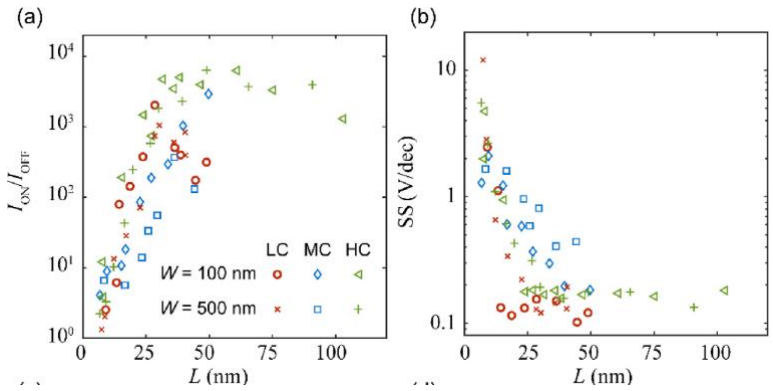


Figure 2. GNR channel length dependence of I_{ON}/I_{OFF} ratio (**a**) and the subthreshold swing, SS (**b**). V_{DS} = –1 V and –0.1 V in (a) and (b), respectively.

Recent work has focused on connecting specific nanomaterial morphologies with device performance to understand the scaling trends of bottom-up synthesized GNR transistors.[NG6] Using a combined theoretical and experimental approach, the

effects of the GNR spatial distributions, the GNR-GNR relocation and bundling during the device fabrication processes, and the overlaps between the metal contacts and the GNR channel were quantitatively investigated. Key findings include: 1) Dramatic increases of both I_{ON} and device yield as the channel length (L) is downscaled. 2) Strong correlation between the gate coupling efficiency with the channel length, as suggested by the scaling trends for both the I_{ON}/I_{OFF} ratio and the subthreshold swing (SS) (Figure 2a and b, respectively). 3) Improvement of the source/drain metal contact to the GNR channel for longer GNR samples.

In addition, in collaboration with researchers from Switzerland and Germany, the **Bokor** group also performed a broad study on growth optimization of narrow-bandgap GNRs and their integration into functioning devices.[NG7] The team uncovered optimized chemical synthesis conditions resulting in the formation of 5-atom wide armchair GNRs (5-AGNRs) with significantly increased length (up to 45 nm). As a result, the GNRs could be successfully integrated into field effect transistor devices with a fabrication yield of 82%. The team also investigated the impact of GNR alignment on device performance. For this, two high coverage 5-AGNRs samples were fabricated, one using uniaxially aligned 5-AGNRs achieved through growth on an Au(788) substrate with narrow (111) terraces, and one using randomly oriented 5-AGNRs grown on an Au(111)/mica substrate. The comparison (Figure 3, bottom) shows that the device with aligned GNRs exhibits significantly higher ON-state performance resulting in I_{ON}/I_{OFF} ratios exceeding 10^3, the highest reported value for this type of GNRs.[NG7]

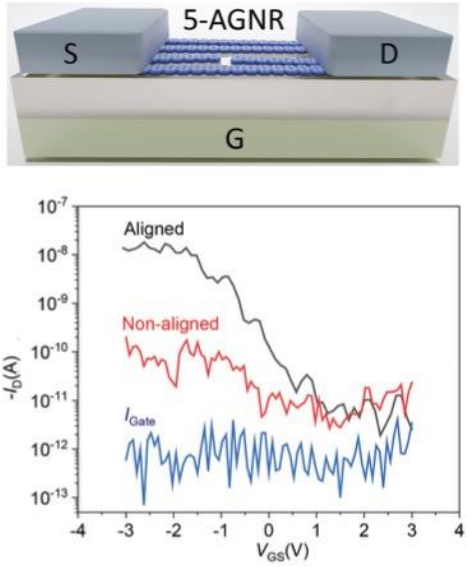


Figure 3. Top. Schematic of an FET device with bottom-up synthesized 5-AGNRs fabricated on HfO_2 gate dielectric and tungsten local bottom gate with palladium electrodes. **Bottom.** I_D vs. V_{GS} characteristics of aligned and non-aligned 5-AGNR FETs at room temperature (V_{DS} = −1 V).

B. Low-Temperature Semiconductor Processing

The **Javey** group is leading the BETR Center's research activities in 2D semiconductors and processing of high-quality semiconductors at near-ambient temperatures. The latter has become increasingly important for both transparent/flexible electronics and monolithic 3D-CMOS architectures. While several solutions exist for n-type semiconductors, low-temperature fabrication of high-quality p-type semiconductors is still challenging. A breakthrough in this regard was recently reported by the **Javey** group by successful thermal evaporation of tellurium thin films at cryogenic temperatures.[NG8, NG9] The group performed in-depth studies on the kinetics and dynamics of the crystallization of thermally evaporated films of single-crystal tellurium with a lateral dimension of up to 6 μm on various substrates including glass and plastic. Moreover, field effect transistors (FETs) fabricated with these tellurium films exhibited a typical p-type characteristic with remarkable subthreshold swing of 2.7 V dec^{-1}, excellent effective hole mobility of 93 cm^2/Vs, and ON/OFF current ratios of $\approx 10^5$ at room temperature.[NG8]

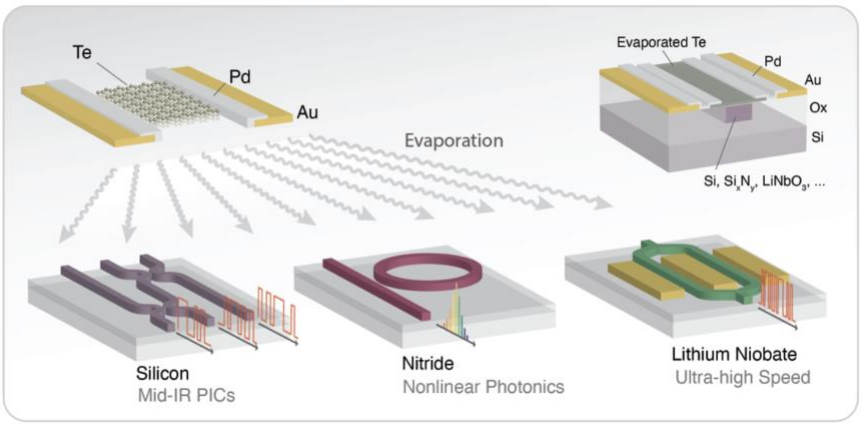


Figure 4. Schematic of tellurium photodetector devices, including applications as mid-IR photonic integrated circuits, nonlinear photonics, and ultra-high-speed devices.

In this period, the **Javey** group partnered with colleagues at Stanford University to demonstrated scalable integration of low-temperature thermally evaporated tellurium films directly onto photonic chips to form air-stable, high-speed, ultrawide-band photo-detectors.[NG10] This approach directly addresses the lack of integrated photodetectors in photonics platforms due to inherent material incompatibilities and lack of process scalability. The high mobility of evaporated tellurium resulted in state-of-the-art device bandwidths of more than 40 GHz. The team showed that these detectors can be fabricated on a variety of novel PIC platforms (including silicon, silicon nitride, and lithium niobate), and the small bandgap of the evaporated tellurium allows for operation from the visible to the mid-IR (Figure 4).

C. Novel Switches and Memory Approaches Based on NEM Relays

A breakthrough toward widespread application of non-volatile nano-electromechanical (NEM) switches (or relays) for next-generation computing was demonstrated in the **Liu** group by monolithically integrating them wit h CMOS circuitry, using multiple metallic layers in the BEOL stack of a standard 65nm CMOS process, followed by a release etch after CMOS fabrication.[NG11] Pioneered by the **Liu** group, non-volatile NEM switches use electrostatic force to mechanically actuate a movable structure to make or break physical contact between current-conducting electrodes. Importantly, when the electrodes are separated physically by an air gap, no current flows across the gap, resulting in zero OFF-state current. Hence NEM switches have abrupt ON/OFF switching characteristics, in addition to robust operation across a wide temperature range, down to cryogenic temperatures, and are excellent candidates for energy efficient computing.[NG12,NG13]

In parallel, the **Liu** group continued to explore system-based integrated circuit implementations in the so-called "edge computing" scenarios, including arrays of reconfigurable NEM-based interconnects for novel memory applications.[NG14] In this period, the group introduced an entire new approach to use reconfigurable NEM-based interconnects as non-volatile memory devices through controlled contact welding and unwelding.[NG15] They showed that MEM switches designed for digital logic applications can be used as multi-time programmable via controlled contact welding and unwelding (Figure 5). The MEM switches were programmed and erased with relatively small voltage (< 3V) and that they displayed excellent retention characteristics. In fact,

reprogrammability with consistently low programmed state resistance, and excellent (essentially infinite) retention time was demonstrated at elevated temperatures (200 °C). This newfound capability provides for greater versatility of device operation, enabling non-volatile information storage to be embedded with digital logic circuitry with no incremental fabrication cost. Considering that MEM logic circuits can operate with high energy efficiency and zero standby power, and that the fabrication process for MEM switches is relatively simple and can be compatible with a variety of substrates including plastic, these results affirm that MEM switches are attractive for applications such as the Internet of Things and wearable or disposable electronics that require ultra-low power consumption as well as relatively low manufacturing cost.

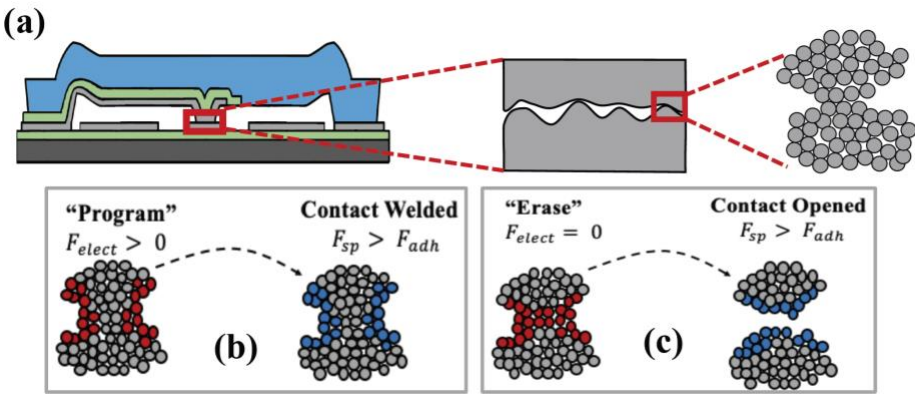


Figure 5. Contact welding and unwelding in a MEM switch: **a.** Due to surface roughness, on-state conductance occurs through one or more contacting asperities. **b.** During "Program" operation and after program showing effectively welded contacting electrodes. **c.** During "Erase" operation and after erase showing opened contact.

D. Ultrafast Magnetic Switching

The **Bokor** and **Salahuddin** groups are developing current-driven, ultra-high speed magnetic elements for logic and memory with switching energies at the sub-femtojoule level.[NG3,NG16] Magnetic systems are attractive logic switches since their non-volatility can be used to reduce static power losses. However, the low speed of magnetic switching has severely limited device applications. The BETR research team demonstrated that ultrafast switching of magnetic materials is possible by hot electrons that are excited via electrical pulses from photoconductive switches.[EM4] Subsequently, the group demonstrated spin-orbit torque (SOT) switching of a ferromagnet with picosecond electrical pulses,[NG16] and ultrafast switching of exchange coupled ferromagnet-ferrimagnet heterostructures.[NG17]

In this period, **Bokor** group performed an in-depth study to gain deeper insights into the phenomenon of helicity-independent all-optical magnetization switching (HI-AOS) in an exchange coupled ferromagnet–ferrimagnet (FM-FEM) heterostructure (Figure 6).[NG18] Using a modified microscopic three-temperature model, the team investigated the effect of (i) the Curie temperature of the FM, (ii) the FEM composition, (iii) the long-range Ruderman-Kittel-Kasuya-Yosida (RKKY) exchange-coupling strength, and (iv) the absorbed optical energy on the element-specific time-resolved magnetization dynamics. This analysis demonstrated that the threshold switching energy depends on the composition of the FEM and the switching time depends on the Curie temperature of the FM as well as RKKY coupling strength. The results of this study pave the path to developing faster and more energy-efficient spintronics devices.

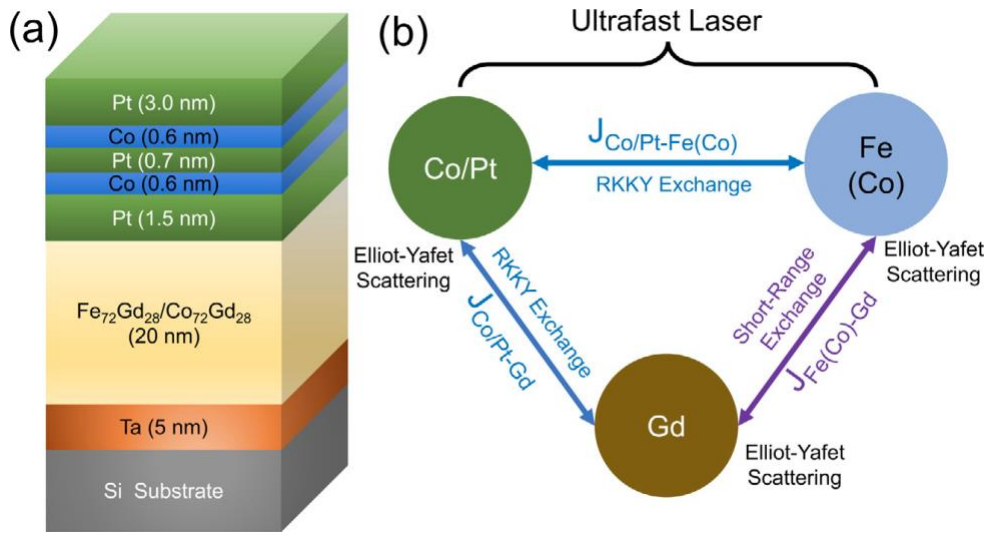


Figure 6. a. Schematic diagram of the exchange-coupled heterostructure. **b.** Depiction of the different types of exchange interactions acting on the sub-lattices of the sample.

2.2.2 Current Projects

NEM Switches Monolithically Integrated with CMOS Circuitry

(Prof. Tsu-Jae King Liu)

Nanoelectromechanical (NEM) switches can be operated at ultralow voltages (<20 mV) and have abrupt ON/OFF switching characteristics, in addition to robust operation across a wide temperature range. Taking advantage of ultra-scaled interconnect pitch in state-of-the-art CMOS technology, the team demonstrated that vertical non-volatile NEM switches can be implemented using multiple interconnect layers in the back-end-of-line (BEOL) stack of a standard 16 nm CMOS process. Such integrated systems have enormous potential for CMOS power gating, configuration of field-programmable gate arrays, non-volatile back-up storage of information in SRAM and CAM cells, and energy-efficient, fast and reconfigurable look-up tables. Current projects focuss on demonstration of BEOL NEM switches at extreme temperature conditions and on technology scaling to achieve programming voltage of NEM switches in the range compatible with standard I/O CMOS circuitry.

Monolithic 3D CMOS

(Prof. Ali Javey)

The Javey group has been exploring new materials and process schemes to enable synthesis of high electronic grade semiconductors at very low temperatures to enable monolithic 3D CMOS. That has been the primary challenge in achieving such architectures. They have developed a new growth mode, where single crystalline structures of III-V's and tellurium can be grown on any

substrate, including amorphous oxides at ~200 °C with high carrier mobility. Current work aims at exploring to advance the use of this platform for back-end electronics and 3D CMOS.

On-Chip Ultrafast Magnetic Switching

(Profs. Jeffrey Bokor, Sayeef Salahuddin, Vladimir Stojanović)

This project builds on the recent breakthrough of ultrafast spin-orbit torque (SOT) switching of a ferromagnet with picosecond electrical pulses.[NG16] Currently, the team is exploring on-chip ultrafast magnetic switching and readout triggered by electrical pulses generated directly by CMOS circuits. Conventional CMOS scaling is projected to reach transistor speeds in the range of a few picoseconds, so such electrical pulses will be available on-chip. To take advantage of this technology, the team works on integrating magnetic device structures on advanced CMOS chips. Two challenges have to be overcome toward this goal: (1) Integration of an electrical readout into the circuit structure, and (2) reduction of both the switching energy and current to be compatible with CMOS technology. In fact, calculations revealed that energies and currents for the electrical switching of magnets could be as low as ~3.5 fJ and ~10's of μA, respectively, for a $(20\ nm)^3$ cell size.

In-Memory and Normally-Off Computing Using Magnetic Nonvolatile Devices

(Profs. Jeffrey Bokor, Sayeef Salahuddin, Vladimir Stojanović)

This project focuses on the fabrication, design, and integration of in-memory and normally-off computing using magnetic nonvolatile devices with the goal of integrating three-terminal spin-Hall memory devices with a CMOS latch. The basic idea has been to reduce power by turning off large portions of the computer that are not in use. By using non-volatile memory, the shut-down part of the computer can readily be restored to its original state, once it is needed, without needing to write to or read from external storage. By distributing the memory over the circuit (memory-in-logic), additional power savings due to reduced interconnect length can be expected. Several spin-based devices added to SRAM circuits were evaluated and analysis across a number of various benchmarks promises 35 percent energy savings with this type of memory.

2.2.3 Publications (Next-Generation Devices – NG)

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NG8. C. Zhao, C. Tan, D.H. Lien, X. Song, M. Amani, M. Hettick, H.Y.Y. Nyein, Z. Yuan, L. Li, M.C. Scott, and A. Javey, "Evaporated Tellurium Thin Films for p-type Field-Effect Transistors and Circuits," *Nature Nanotechnology*, vol. 15, pp. 53-58, Jan 2020.
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NG11. U. Sikder, G. Usai, T.-T. Yen, K. Horace-Herron, L. Hutin, and T.-K. Liu, "Back-End-of-Line Nano-Electro-Mechanical Switches for Reconfigurable Interconnects," *IEEE Electron Device Letters*, vol. 41, pp. 625-628, Apr 2020.
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NG14. K. Kato, V. Stojanović, and T.-J. K. Liu, "Embedded Nano-Electro-Mechanical Memory for Energy-Efficient Reconfigurable Logic," *IEEE Electron Device Letters*, vol. 37, pp. 1563–1565, Dec. 2016.
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2.3 Thrust 2: Flexible and Wearable Electronics

The goal of the Wearable and Flexible Electronics research projects in the BETR Center is to develop a new manufacturing and deployment paradigm for wearable, interactive information devices, including displays, sensors, and logic devices. Research activities are guided by the recognition that electronic devices must be non-intrusive, easily deployed and inexpensive, to become a pervasive technology. Spearheaded by the research groups of **Prof. Ali Javey** and **Prof. Ana Arias**, wearable and flexible electronics research in the BETR Center entails the development of tools, processes and materials for roll-to-roll processing, layer transfer, high-resolution printing, thin-film development, and packaging.[FE1,FE2] An excellent overview on recent developments in wearable biosensing is given in the *ACS Nano* multi-PI review article "Technology Roadmap for Flexible Sensors", co-authored by **Prof. Javey.**[FE3]

2.3.1 Recent Achievements

A. Wearable Electronics for Sweat Monitoring

Monitoring sweat secretion rate is essential for uncovering underlying physical conditions like hyperhidrosis, mental stress, and neural disorders. The **Javey** group has pioneered the design and fabrication of wearable electronic patches for continuous sweat monitoring using its expertise in microfluidics.[FE4] The microfluidic design combats evaporation, enable selective monitoring of secretion rate, and reduce required sweat accumulation times. The group also presented wearable sweat sensors with convenient glove-based form factors for sweat sensing under routine and even sedentary activity, making sweat-based biomarker monitoring practical for daily life.[FE5] Typically, flexible microfluidic sweat rate monitoring devices use tape as a means of attachment to the skin to tightly seal the collection area. This, however, complicates their potential integration with available commercial wearables, such as smartwatches.

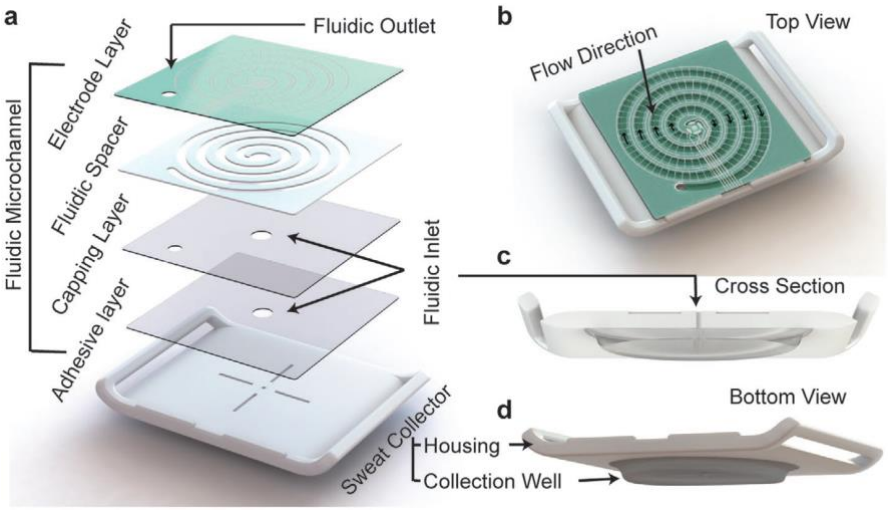

Figure 7. Tape-free 3D printed wearable sweat rate monitoring device. **a.** Layer-by-layer stack of the device structure. **b.** Top view of the device showing the face-to-face comb-like electrode for admittance measurement. **c.** A cross-sectional view of the sweat collector showing a common fluidic inlet between the soft sweat collector and the hard housing. **d.** A bottom view of the skin interfacing sweat collection well.

In this period, the **Javey** group introduced a tape-free device, consisting of a 3D-printed sweat collector with a concave surface that is

strapped onto the skin to form an effective seal (Figure 7).[FE6] The materials, structure, and dimensions of the sweat collector were optimized for conformal device-to-skin contact and efficient capture of sweat. The collector is interfaced with a fluidic microchannel with embedded electrodes for continuous digital monitoring of sweat rate. Long-term exercise-induced local sweat rate from multiple body locations in both multi-subject and longitudinal studies was measured, depicting the correlation between the measured sweat profile and total body fluid loss. The simple installation procedure and reusability of this tape-free device make it a good candidate for integration with the band of a watch.

B. Flexible Devices for Magnetic Resonance Imaging

The **Arias** group is developing various device fabrication methods based on roll-to-roll printing (screen and inkjet printing), blade coating, and organic binding techniques. For example, the group developed printed flexible composite Zn/MnO_2 batteries using organic gels as binder for the MnO_2 electrode,[FE7] and fully flexible ambient light pulse oximeters from new organic photodiodes compatible with roll-to-roll printing techniques.[FE8] Recently, the **Arias** group (in collaboration with EECS Professor Michael Lustig) developed a digital fabrication method for custom MRI receive coils using a vacuum forming and electroless copper plating approach.[FE9] With this new process, it was possible to fabricate intricate copper traces on curved surfaces so that coil arrays place the receivers as close to the body as possible (Figure 8). In short, a three-dimensional scan of a desired anatomy was obtained first and used to design the coil elements. The layout is pre-distorted with a self-built simulation of the vacuum forming process and the desired coil geometry is then patterned onto a polycarbonate sheet by sandblasting through a tape mask. The sandblasted areas are catalyzed with a palladium-tin solution and vacuum formed. The catalyzed part is then placed into a custom-built plating tank and copper plated. This work presents the first example of vacuum formed coils with direct electroless copper plating and will enable the rapid development of a set of coils of different sizes for new MRI applications.

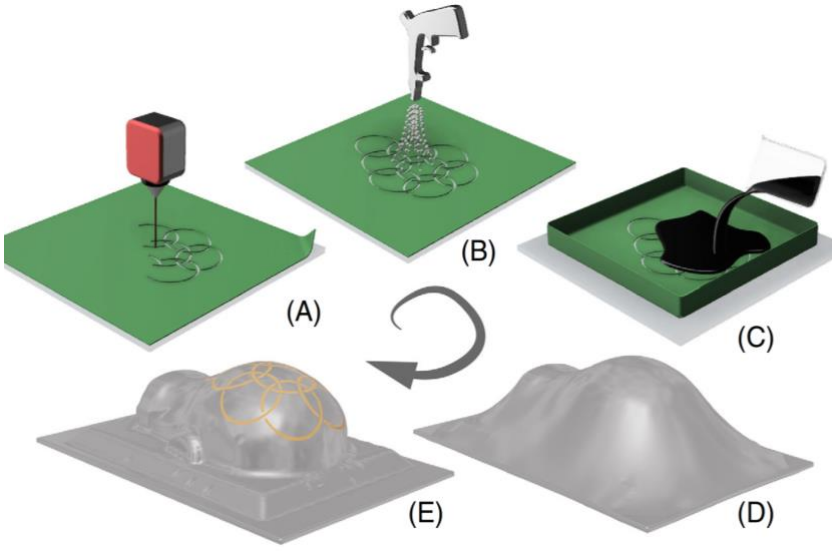

Figure 8. (A) A polycarbonate sheet is masked with polyester tape and the pre-distorted coil pattern is cut out of the mask with a CO2 laser. **(B)** The sheet is sandblasted with 100 grit white fused aluminum oxide. **(C)** After cleaning, the exposed areas are catalyzed with a palladium-tin solution. **(D)** The mask is removed, and the sheet is vacuum formed. **(E)** The vacuum formed plastic is removed from the mold and copper plated in an aqueous solution of copper sulfate, ethylenediaminetetraacetic acid, sodium hydroxide, and formaldehyde.

Collaborating with Prof. Lustig, the **Arias** group also designed novel caterpillar cable traps for MRI applications.[FE10] These new traps provide sufficient attenuation to shield currents while allowing cable flexibility. The samples were fabricated with toroids and spacers using injection molding of a low-loss polydimethylsiloxane (PDMS) elastic substrate. A mold with wire slits was 3D printed and used for injection molding (Figure 9A and B). The molded toroids can be wound with a 28 AWG wire (Figure 9C). A stiff PDMS substrate was chosen for the resonant toroids, whereas a more flexible substrate was used for the spacers. This enables flexibility of the overall structure with little geometric variation of the toroidal traps because most of the stress and deformation is applied to the softer material. The team showed that the new distributed design can provide high blocking efficiency at different positions and orientations, even in cases where commercial cable traps cannot.

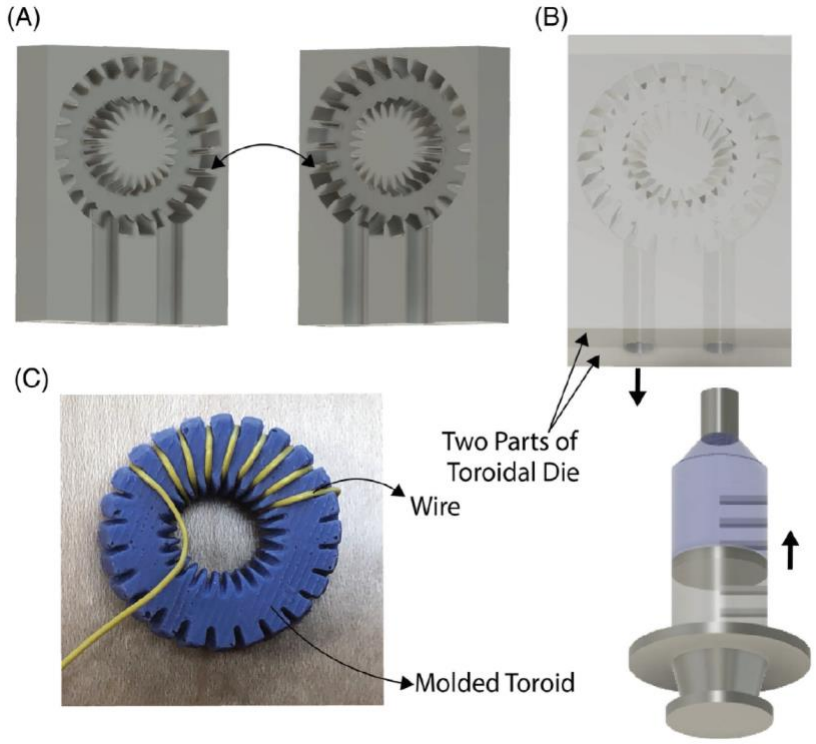

Figure 9. Fabrication process of the toroids. **(A)** A mold with two parts is designed and 3D-printed. **(B)** The two parts of the mold are clamped together. The PDMS mixture is injected into the mold using a syringe and left to cure. **(C)** The cured toroid is removed from the mold, and the slits on the toroid are used to wind the wire. PDMS, polydimethylsiloxane.

2.3.2 Current Projects

Wearable Sensors for Non-Invasive Continuous Monitoring of Biomarkers
(Prof. Ali Javey)

The goal of this proposal is to develop non-invasive sensors that can continuously monitor the concentrations of clinically relevant biomarkers in readily accessible bodily fluids, such as sweat.[FE1,FE3,FE4] The sensors will be used to perform medium to large scale population studies with vast time-series of data to generate personalized baselines indicative of the user's health. Over the last several years, the Javey group has developed a portfolio of wearable electrochemical sensors generally consisting of two main components that are interfaced together: (i) disposable sensor patch, and (ii) reusable electronics for signal condition, processing and transmission. They have

developed roll-to-roll fabrication schemes for the sensor patches to enable a cost-effective method of mass producing the sensors through our collaboration with external partners, including VTT. The group has demonstrated small scale population studies to observe preliminary correlations for certain analytes, including pH, Cl^-, Na^+, vitamin C, nicotine, caffeine, and levodopa.

2.3.3 Publications (Flexible Electronics – FE)

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FE2. Y. Khan, A. Thielens, S. Muin, J. Ting, C. Baumbauer, and A.C. Arias, "A New Frontier of Printed Electronics: Flexible Hybrid Electronics," *Advanced Materials*, vol. 32, pp. 1905279, Apr 2020.

FE3. J. Luo, A. Javey, et al., "Technology Roadmap for Flexible Sensors," *ACS Nano*, vol. 17, pp. 5211-5295, Mar 2023.

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2.4 Thrust 3: Hardware Accelerators for AI

The recent explosion of machine learning, neural networks, and other artificial intelligence applications goes hand in hand with growing demands for new hardware architectures. New machines for solving difficult combinatorial optimization problems are needed since the conventional von-Neumann computer is ill-suited for most applications in terms of latency and energy efficiency. The intrinsic architectural and algorithmic limitations of traditional computers open the door for alternative physical systems based on emerging technologies. The BETR Center research groups of **Professors Sayeef Salahuddin**, **Sophia Shao, Vladimir Stojanović**, and **Eli Yablonovitch** address this very challenge by investigating hardware accelerators specialized for large-scale matrix computations used in machine learning and deep neural networks.[AI1-AI4] BETR Center researchers develop solutions for deep neural networks based on novel logic switches, architecture-aware network pruning techniques, systematic optimization strategies of deep learning architectures, and analog machines that can solve NP-hard optimization problems without the need for the complexity of quantum bits.

2.4.1 Recent Achievements

A. New Strategies for AI Accelerator Design

Accelerator hardware design space exploration is a challenging problem due to its intractable high-dimensional search space with many different design parameters, many of which cannot be made independently as they have intricate interactions with each other. Central to this problem is the intractable search complexity that grows exponentially with the design choices and the discrete nature of the search space. The **Shao** group addresses this challenge by exploring the feasibility of learning a meaningful low-dimensional continuous representation for hardware designs to reduce such complexity and facilitate the search process.[AI5] The group devised a variational autoencoder (VAE)-based design space exploration framework called VAESA, to encode the hardware design space in a compact and continuous representation (Figure 10). The team showed that black-box and gradient-based design space exploration

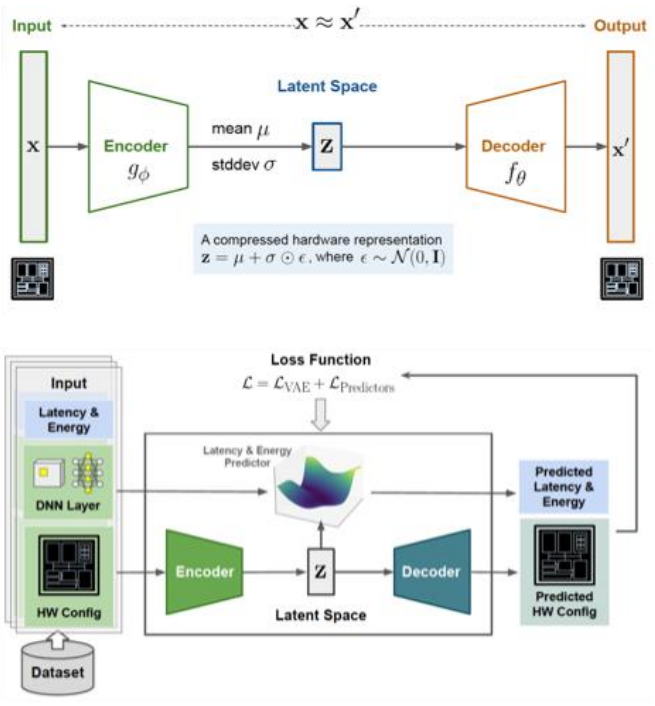

Figure 10. Top: Example variational autoencoder (VAE) model to learn a low dimensional representation **z** for hardware design. **Bottom:** The VAESA training pipeline to learn the latent space of hardware design. The dataset includes the latency and energy costs of DNN layers running on different DNN accelerator architectures.

algorithms can be applied to the latent space, and design points optimized in the latent space can be reconstructed to high-performance realistic hardware designs. Our experiments show that performing the design space search on the latent space consistently leads to the optimal design point under a fixed number of samples. In addition, the latent space can improve the sample efficiency of the original algorithm by 6.8 times and can discover hardware designs that are up to 5% more efficient than the optimal design searched directly in the high-dimensional input space.

B. Domain-Specific Accelerator Design

The **Yablonovitch** group explores physical machines, which can solve optimization problems by employing the maximization or minimization principles that are built into physics. In this period, the group introduced a dynamical solver for the Ising problem that is comprised of a network of coupled bistable parametric oscillators and they showed that it implements Lagrange multiplier constrained optimization (Figure 11).[AI6] In detail, the team demonstrated that the 2ω pump depletion effect, which is intrinsic to parametric oscillators, automatically enforces the binary Ising constraints, enabling the system's continuous analog variables to converge to high-quality binary solutions to the optimization problem. Moreover, an exact correspondence between the equations of motion for the coupled oscillators and the update rules in the primal-dual method of Lagrange multipliers was established. While the analysis was performed using electrical LC oscillators, it can be generalized to any system of coupled parametric oscillators. By simulating the dynamics of the coupled oscillator system on benchmark problems they demonstrated that its performance is comparable with the best-known results.

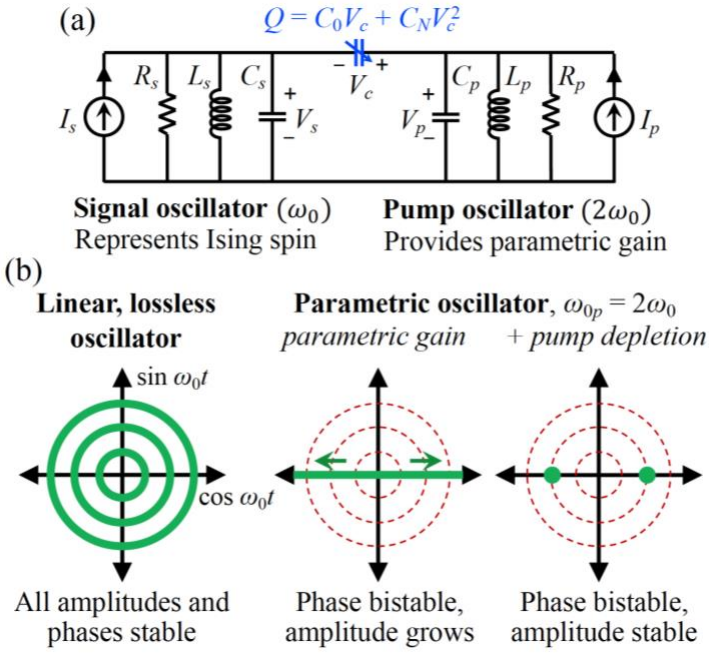

Figure 11. Top: Parametric LC oscillator circuit, consisting of a signal and pump oscillator connected by a nonlinear capacitor. (b) A linear, lossless LC oscillator (left) can support oscillations of any phase and any amplitude. A parametric LC oscillator (right) supports oscillations only at two phases separated by π rad as a result of parametric amplification. Pump depletion further constrains the amplitude to be monostable.

C. Memory-Centric Adaptive Accelerator Architecture

To address the wide adoption of deep neural networks (DNNs) across different application domains, multi-tenancy execution, where multiple DNNs are deployed simultaneously on the same hardware, has been proposed to satisfy the latency requirements of different applications while

improving the overall system utilizatio n. However, multi-tenancy execution could lead to undesired system-level resource contention, causing quality-of service (QoS) degradation for latency-critical applications. The **Shao** group has addressed this very challenge by proposing, implementing, and analyzing an adaptive multi-tenancy system for DNN accelerators, named MoCA.[AI7] Unlike existing solutions that focus on compute resource partition, MoCA dynamically manages shared memory resources of co-located applications to meet their QoS targets. Specifically, MoCA leverages the regularities in both DNN operators and accelerators to dynamically estimate and manipulate the usage of memory resources based on their latency targets and user-defined priorities so that co-located applications get the resources they demand without significantly starving their co-runners (Figure 12, top). The group demonstrated that MoCA improves the satisfaction rate of the service level agreement (SLA) up to 3.9 times (1.8 times average), system throughput by 2.3 times (1.7 times average), and fairness by 1.3 times (1.2 times average), compared to prior work (Figure 12, bottom). Importantly, MoCA provides these benefits while incurring less than 1% area overhead of a state-of-the-art DNN accelerator.

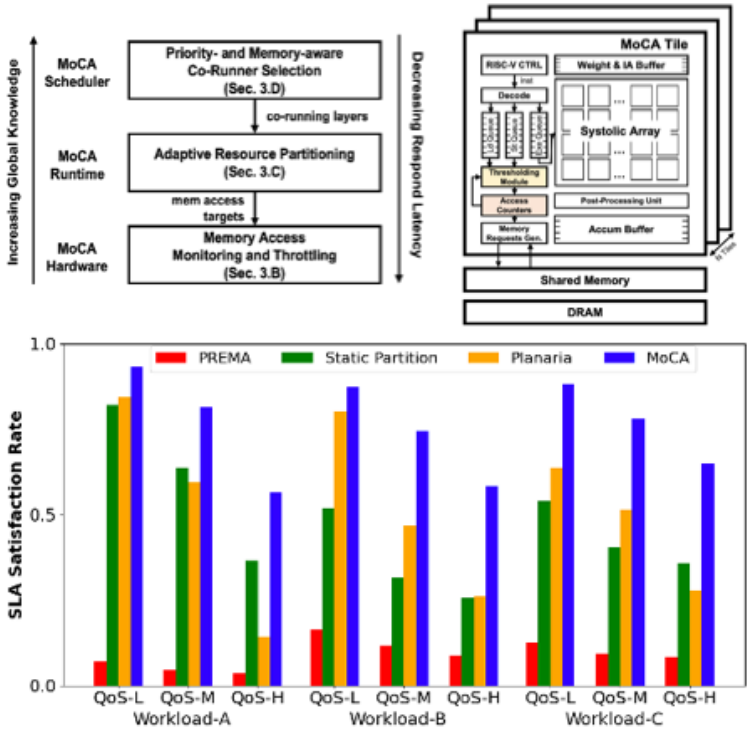

Figure 12. Top. Overview of the MoCA system (left) and schematic of the MOCA DNN accelerator that supports dynamic memory access monitoring and throttling. **Bottom.** MoCA's SLA satisfaction rate improvement over multitenancy baselines with different QoS targets.

2.4.2 Current Projects

Photonic and Analog-Mixed Signal Generators

(Prof. Vladimir Stojanović)

The Stojanović group is developing design automation tools for photonic and AMS design. Berkeley Photonic Generator has been developed to streamline the design and optimization of complex layout shapes needed for silicon-photonic designs for various applications. It plugs directly into the Berkeley Analog Generator framework enabling photonic-ams co-design. The BPG framework is open-source and contains generator libraries for a large array of silicon-photonic components. The generator is structured in a way to support compilation of the photonic

components into different foundry process kits, from the same generator base. They are also developing AI/ML based design automation methods on top of BAG to enable AMS circuits process porting and topology optimization.

Physics-Based Digital Optimization

(Prof. Eli Yablonovitch)

Optimization is vital to engineering, artificial intelligence, control theory and many areas of science. Mathematically, we usually employ steepest-descent, or other digital algorithms, however, physics itself, performs optimizations in the normal course of dynamical evolution. Nature provides us with the following optimization principles: (1) The Principle of Least Action; (2) The Variational Principle of Quantum Mechanics; (3) The Principle of Minimum Entropy Generation; (4) The First Mode to Threshold Method; (5) The Principle of Least Time; (6) The Adiabatic Evolution Method; (7) Quantum Annealing. In effect, physics can provide machines which solve digital optimization problems much faster than any digital computer. Of these physics-based principles, "Minimum Entropy Generation" in the form of bistable electrical or optical circuits is particularly adaptable toward offering digital optimization.

Accelerator Integration

(Prof. Sophia Shao)

The Shao group is developing systematic methodologies and optimizations to enable efficient accelerator integration with the rest of System-on-Chip and/or System-in-Package. The goal is to holistically understand the system-level interactions across accelerators, general-purpose cores, and shared resources so that they can efficiently execute a wide range of applications in future-generation of SoCs and SiPs.

Accelerator Programming Infrastructure

(Prof. Sophia Shao)

The Shao group is building high-productivity programming infrastructure to enable fast and efficient mapping of applications to domain-specific systems. In particular, they leverage the regularity in both applications and domain-specific systems and formulate the programming problems as a constrained-optimization problem.[AI8] The group demonstrated that by leveraging advances in integer-linear programming and deep reinforcement learning, they can quickly find performant scheduling solutions without going through expensive, brute-force search.

Stochastic Neural Networks Based on Restricted Boltzmann Machines

(Prof. Sayeef Salahuddin)

The Salahudding group recently demonstrated that a restricted Boltzmann machine (RBM) can solve NP-Hard combinatorial optimization problems by exploiting the intrinsic parallelism present in the RBM architecture on a flexible Field Programmable Gate Array (FPGA) based accelerator.[AI9] The goal of this project is to show that further accelerator-level parallelization and scaling are possible through the use of multi-FPGA designs and communication, time division multiplexing, and more efficient pipeline stages. This will open the possibility of using parallel,

stochastic computing to solve NP-Hard and NP-Complete problems with far reaching consequences in fields like logistics, scheduling, resource allocation, and many others.

2.4.3 Publications (Artificial Intelligence – AI)

AI1. L. Supic, R. Naous, R. Sredojevic, A. Faust, and V. Stojanović, "MPDCompress - Matrix Permutation Decomposition Algorithm for Deep Neural Network Compression," *arXiv*:1805.12085, May 2018.

AI2. S. K. Vadlamani, T. P. Xiao, and E. Yablonovitch, "Physics Successfully Implements Lagrange Multiplier Optimization," *Proceedings of the National Academy of Sciences*, vol. 117, no. 43, pp. 26639-26650, Oct 2020.

AI3. M. Kellman, M. Lustig, L. Waller, "How to do Physics-based Learning," *arXiv*:2005.13531, May 2020.

AI4. K. Hakhamaneshi, N. Werblun, P. Abbeel, and V. Stojanovic, "BagNet: Berkeley Analog Generator with Layout Optimizer Boosted with Deep Neural Networks," *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA, 2019, pp. 1-8, Jan 2020.

AI5. Q. Huang, C. Hong, J. Wawrzynek, M. Subedar, and Y. S. Shao, "Learning A Continuous and Reconstructible Latent Space for Hardware Accelerator Design," *2022 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Singapore, Singapore, pp. 277-287, May 2022.

AI6. S. K. Vadlamani, T. P. Xiao, and E. Yablonovitch, "Equivalence of coupled parametric oscillator dynamics to Lagrange multiplier primal-dual optimization," *2022 IEEE International Conference on Rebooting Computing (ICRC)*, San Francisco, CA, pp. 45-50, Dec 2022.

AI7. S. Kim, H. Genc, V. V. Nikiforov, K. Asanović, B. Nikolić, and Y. S. Shao, "MoCA: Memory-Centric, Adaptive Execution for Multi-Tenant Deep Neural Networks," *2023 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Montreal, QC, Canada, pp. 828-841, Feb 2023.

AI8. Q. Huang, A. Kalaiah, M. Kang, J. Demmel, G. Dinh, J. Wawrzynek, T. Norell, and Y. S. Shao, "CoSA: Scheduling by Constrained Optimization for Spatial Accelerators," *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA)*, pp. 554-566, Aug 2021.

AI9. S. Patel, P. Canoza, and S. Salahuddin, "Logically Synthesized and Hardware-Accelerated Restricted Boltzmann Machines for Combinatorial Optimization and Integer Factorization," *Nature Electronics*, vol. 5, pp. 92-101, Feb 2022.

2.5 Thrust 4: System Integration

Future information and communication (ICT) applications set a broad context for research conducted in the BETR Center research groups of **Professors Tsu-Jae King Liu**, **Sophia Shao**, and **Vladimir Stojanović**. While system integration research efforts in the BETR Center are complementary to other industry-sponsored centers such as the Berkeley Wireless Research Center (BWRC), collaborative projects with BWRC serve to bridge innovations in physical electronics together with innovations in IC design, for co-optimization of new solid-state device technologies and computer architectures.[SI1-SI4] Through device modeling and simulation of integrated systems, tradeoffs between energy efficiency and performance can be optimized for a wide range of applications.

2.5.1 Recent Achievements

A. Ultrafast Electronic-Photonic Egress Link

While quantum computing has been gaining ground in recent years, two key challenges in scaling toward a large quantum system-on-chip (QSoC) with arrays of stochastic photon-pair sources are 1) to maintain the same wavelength for each source, which is necessary for preventing quantum decoherence and qubit errors, and 2) to isolate the photon pairs from the strong classical pump light. While pair sources with either frequency locking or high-extinction pump filters have been demonstrated, this was not done simultaneously on the same chip, nor have on-chip electronics been used to produce modular units for scalable QSoCs.

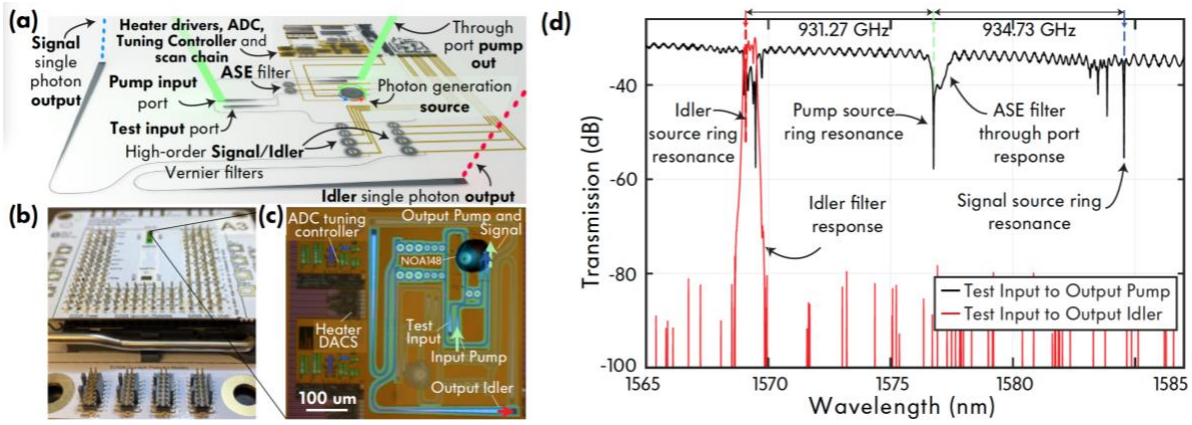

Figure 13. a) EPQSoC schematic. **b)** CMOS package with chip carrier and host board. **c)** EPQSoC micrograph. **d)** Idler output port and through port transmission from test input port.

To address these issues, the **Stojanović** group (with colleagues at MIT) developed the first electronic-photonic quantum system-on-chip (EPQSoC).[SI5] This new system is aimed toward the function of a self-contained, "wall-plug" photon-pair source on chip. The eventual goal is for this device to accept only DC electrical power and CW pump-laser light ("optical power") and output quantum-correlated photon pairs. The current work enables a spontaneous four-wave mixing (SFWM) photon-pair source, which combines feedback-controlled frequency locking, high

extinction (>80 dB) on-chip pump filtering, and signal/idler demultiplexing with circuits implemented alongside photonics in a 45 nm SOI CMOS platform (Figure 13). This is the same platform the team used previously to demonstrate large-scale electronic-photonic.[SI6]

B. Relay-Based Digital Integrated Circuits

The **Liu**, in collaboration with the **Stojanović** group, has demonstrated reliable operation of relay-based digital integrated circuits (ICs) with 50 mV supply voltage.[SI2,SI3] No other digital IC device technology developed to date has even been projected to be able to operate at such low voltages at room temperature. Recently, the team developed a method to fabricate back-end-of-line (BEOL) non-volatile NEM switches (NV-NEM) switches with minimum (100-nm) contact/actuation gaps, which incorporates a post-foundry release-etch process that is fully compatible with the BEOL material stack.[SI7] The new process enables leveraging multiple CMOS BEOL layers for NEM switches, which is advantageous for achieving lower programming voltage and/or more compact footprint. A functional array of BEOL NV-NEM switches is used to implement a hybrid CMOS-NEM IC for data search applications. Recently, the group also presented a crossbar array architecture of vertically oriented BEOL NV-NEM switches.[SI8]

In this period, the **Liu** and **Stojanović** groups reported a significant advancement by successfully implementing vertically oriented non-volatile NEM switches into a standard 16 nm generation CMOS BEOL process by using multiple metal interconnect layers and corresponding via layers.[SI9] This new generation of switches has a dramatically reduced footprint of only 0.055 μm^2. The team also demonstrated a compact decoder circuit comprising an array of BEOL non-volatile NEM switches and CMOS inverters using 16 nm-node FinFETs (Figure 14). The array of BEOL NEM switches (with four switches spanning 1.6 μm) is much more compact than in previous work (~75 μm; ref. [SI7]). Evaluation of performance improvement with technology scaling reveals that CMOS+NEM technology is promising for future data-centric computing applications.

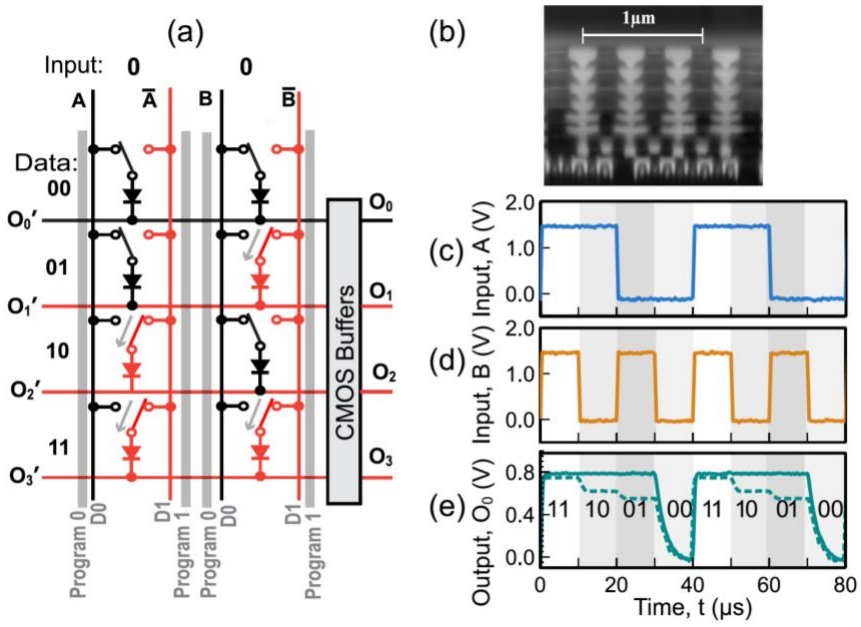

Figure 14. a. Circuit diagram for a CMOS+NEM 2-to-4 line decoder. Lines colored in red indicate wires that are driven to high voltage. **b.** Cross-sectional SEM image showing the four movable beams along a single column of the array. Measured voltage waveforms for the **c-d** input bits and (**e**) output bits demonstrate proper circuit operation.

C. Electronic-Photonic Lab-on-Chip Platform

Recent worldwide challenges to healthcare systems have emphasized the need for accurate and on-demand Point-of-Care (PoC) platforms, which can provide – personalized to each patient – diagnostic and prognostic multiparametric information on various infections. The **Stojanović** group has developed solutions based on electronic-photonic LoC system for biosensing,[SI10-SI12] and recently presented a fully integrated arrayed monolithic electronic-photonic system-on-chip (EPSoC) platform in a zero-change high volume CMOS-SOI process.[SI13]

In this period, the team introduced the first fully integrated 2-D array of electronic-photonic ultrasound sensors targeting low-power miniaturized ultrasound probes for endoscopic applications.[SI14] Fabricated in a zero-change 45-nm CMOS silicon-on-insulator (SOI) technology, this 5.53 × 3.03 mm EPSoC utilizes micro-ring resonators (MRRs) as ultrasound sensors instead of the traditional piezoelectric or capacitive micromachined transducers (Figure 15). The photonic nature of the sensor enables remoting of the power-hungry receive electronics outside the probe tip and eliminates electrical cabling, replacing the bulky micro-coax cables with thinner optic fibers. Leveraging the monolithic integration of photonic devices with CMOS circuitry, a complete receiver unit is built right next to the sensor MRRs, including a programmable gain transimpedance amplifier and background current cancellation digital-to-analog converters, which allow for a sensor operating range of 74 dB. A 9-bit SAR ADC performs on-chip A/D conversion, resulting in a fully self-contained endoscopic ultrasound receiver system.

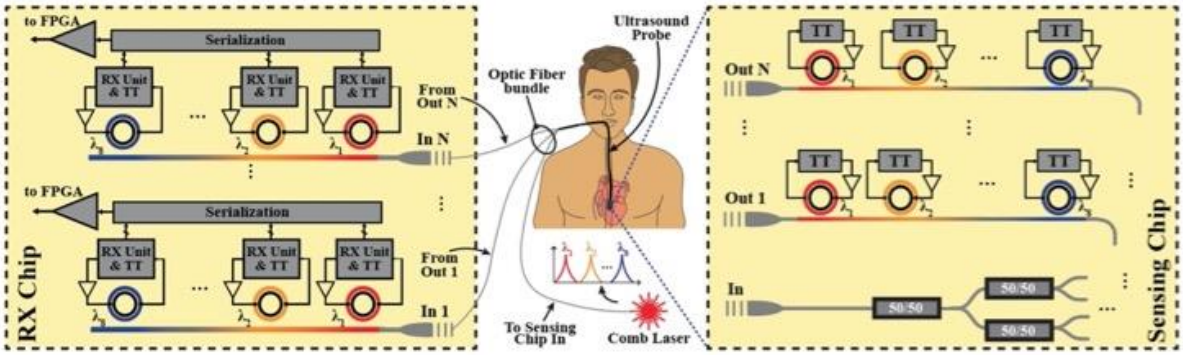

Figure 15. Dual-chip system architecture illustrating the remoted optical ultrasound beamforming array concept for power and area minimization.

2.5.2 Current Projects

SuperFabric

(Prof. Vladimir Stojanović)

SuperFabric looks at design of WDM photonic links that work together with a MEMS-based optical switch (high-radix 128-1024 with sub-us switching time) to aid in scale-out of compute clusters for AI training. The photonic links have fast (sub-100ns) electro-optic wavelength lock and burst-mode CDR and laser forwarding to mitigate switch insertion losses.

mm-Wave Photonic WDM Links for Radar Phase-Array and Massive-MIMO Systems

(Prof. Vladimir Stojanović)

The goal of this project is to design antenna-to-photons analog mm-wave photonic links that minimize the power consumption at the phase-array panel, by converting mm-wave signals from the antenna directly to the optical domain with a mm-wave LNA chain directly modulating ring modulators specialized for mm-wave modulation. The remoted central processing site receivers use coherent demodulation to avoid mm-wave mixers and simplify the mm-wave receiver front-ends.

Relay-Based Digital Integrated Circuits

(Prof. Tsu-Jae King Liu)

Nanoelectromechanical (NEM) relays can achieve immeasurably low off-state leakage and can be operated with much lower voltage swing than any transistor. These devices are therefore excellent candidates for emerging Internet of Things (IoT) applications. Current research aims to demonstrate reliable room-temperature operation of relay-based digital integrated circuits at 10 mV. Key scientific questions that will need to be answered along the way include: 1) What is the fundamental lower limit of operating voltage for mechanical computing? 2) What are key properties of the optimal contact material for milli-Volt mechanical computing? Furthermore, reliable sub-25 mV switching operation of NEM relays was achieved at temperatures below 100 Kelvin. Currently, operation of relays and integrated circuits at temperatures below 1 Kelvin are explored. The goal is to evaluate their compatibility with milli-Kelvin temperatures required for quantum computing.

Cryo-Photonic WDM Links

(Prof. Vladimir Stojanović)

This project aims to design the photonic links that connect superconducting cryo circuits to the outside environment. Superconducting circuits produce signals with 2-4mV amplitudes, which are then converted to optical signals via CMOS pre-amplifier integrated with specialized ring resonator modulators. The link architecture (Coherent Ultrafast Reflective Link - CURL) is a highly asymmetric link to minimize the thermal dissipation in the cryo environment.

Quantum Photonics in CMOS

(Prof. Vladimir Stojanović)

In this project, platform building blocks for the photonic quantum computing are being designed as electronic-photonic systems-on-chip. One of the most complex blocks is the photon pair source that produces correlated photon pairs (through laser modulation and nonlinear filtering) that are used as qubits in linear mixing operations.[SI15] The Stojanović group is also working on developing APDs in the same process for detection of the photon pairs for computation read-out.

2.5.3 Publications (System Integration – SI)

SI1. K. Settaluri, C. Lalau-Keraly, E. Yablonovitch, and V. Stojanović, "First Principles Optimization of Opto-Electronic Communication Links," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 5, pp. 1270-1283, May 2017.

SI2. F. Chen, H. Kam, D. Markovic, T.J. King Liu, V. Stojanovic, and E. Alon, "Integrated Circuit Design with NEM Relays," *Proc. IEEE/ACM ICCAD*, pp. 750-757, Nov 2008.

SI3. Z. A. Ye, S. Almeida, M. Rusch, A. Perlas, W. Zhang, U. Sikder, J. Jeon, V. Stojanović and T.-J. K. Liu, "Demonstration of Sub-50 mV Digital Integrated Circuits with Microelectromechnical Relays," *IEEE International Electron Devices Meeting*, San Francisco, CA, Dec 2018.

SI4. A.H. Atabaki *et al.*, "Integrating Photonics with Silicon Nanoelectronics for the Next Generation of Systems on a Chip," *Nature*, vol. 556, pp. 349-354, Apr. 2018.

SI5. I. Wang, J. M. F. Cabanillas, D. Kramnik, A. Ramesh, S. Buchbinder, P. Kumar, V. Stojanović, and M. A. Popović, "Toward quantum electronic-photonic systems-on-chip: a monolithic source of quantum-correlated photons with integrated frequency locking electronics and pump rejection," *2022 Conference on Lasers and Electro-Optics (CLEO)*, paper SM3N.2, May 2022.

SI6. C. Sun *et al.*, "Single-Chip Microprocessor that Communicates Directly Using Light," *Nature*, vol. 528, pp. 534-538, Dec 2015.

SI7. U. Sikder, K. Horace-Herron, T.-T. Yen, G. Usai, L. Hutin, V. Stojanović, and T.-J. King Liu, "Toward Monolithically Integrated Hybrid CMOS-NEM Circuits," *IEEE Transactions on Electron Devices*, vol. 68, pp. 6430-6436, Dec 2021.

SI8. L. P. Tatum, U. Sikder, and T.-J. K. Liu, "Design Technology Co-Optimization for Back-End-of-Line Nonvolatile NEM Switch Arrays," *IEEE Transactions on Electron Devices*, vol. 68, pp. 1471-1477, Apr 2021.

SI9. U. Sikder, R. Naous, V. Stojanović, and T.-J. K. Liu, "Non-Volatile Nano-Electro-Mechanical Switches and Hybrid Circuits in a 16 nm CMOS Back-End-of-Line Process," *IEEE Electron Device Letters*, vol. 44, pp. 136-139, Jan 2023.

SI10. C. Adamopoulos, S. Buchbinder, P. Zarkos, P. Bhargava, A. Gharia, A. Ninkejad, M. Anwar, and V. Stojanovic, "Fully Integrated Electronic-Photonic Sensor for Label-Free Refractive Index Sensing in Advanced Zero-Change CMOS-SOI Process," *2021 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-2, May 2021.

SI11. P. Zarkos, S. Buchbinder, C. Adamopoulos, S. Madhvapathy, O. Hsu, J. Whinnery, P. Bhargava, and V. Stojanović, "Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Imaging Applications in a Zero-Change 45nm CMOS-SOI Process," *2021 Symposium on VLSI Circuits*, pp. 1-2, Jun 2021.

SI12. C. Adamopoulos, S. Buchbinder, P. Zarkos, P. Bhargava, A. Gharia, A. Niknejad, M. Anwar, and V. Stojanović, "Fully Integrated Electronic–Photonic Biosensor for Label-Free Real-Time Molecular Sensing in Advanced Zero-Change CMOS-SOI Process," *IEEE Solid-State Circuits Letters*, vol. 4, pp. 198-201, Nov 2021.

SI13. C. Adamopoulos, P. Zarkos, S. Buchbinder, P. Bhargava, A. Niknejad, M. Anwar, and V. Stojanović, "Lab-on-Chip for Everyone: Introducing an Electronic-Photonic Platform for Multiparametric Biosensing Using Standard CMOS Processes," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 1, pp. 198-208, Oct 2021.

SI14. P. Zarkos, S. Buchbinder, C. Adamopoulos, S. Madhvapathy, O. Hsu, J. Whinnery, P. Bhargava, and V. Stojanović, "Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Applications in a Zero-Change 45-nm CMOS-SOI Process," *IEEE Journal of Solid-State Circuits*, Early Access, Dec 2022.

SI15. J. M. F. Cabanillas, D. Kramnik, A. Ramesh, C. M. Gentry, V. Stojanović, P. Kumar, and M. A. Popović, "Tunable Source of Quantum-Correlated Photons with Integrated Pump Rejection in a Silicon CMOS Platform," in *Frontiers in Optics + Laser Science 2021*, C. Mazzali, T. (T.-C.) Poon, R. Averitt, and R. Kaindl, eds., *Technical Digest Series (Optica Publishing Group, 2021)*, paper FTu2E.1, Nov 2021.

2.6 Computational Imaging

Computational imaging is an emerging field of metrology, involving the co-design of imaging system hardware and software for optimization across the entire pipeline from acquisition to reconstruction. With this approach, new, computational-imaging-based microscopes can be designed for 3D aberration and phase measurement. Computational imaging research in the BETR Center is led by **Professor Laura Waller**, and it is focused on designing imaging systems and algorithms jointly using simple hardware. The team is also exploring a new direction by not just reconstructing images from a given data set but encoding the information in the hardware and using data-driven approaches to optimize capture of the images and set up of the physical system in conjunction with image reconstruction.[CI1] In the past, the BETR team performed a feasibility study for transferring optical phase measurements for inspection of large optical components in the supply chain of BETR Center industrial affiliate **Lam Research.** The team is also conducting fundamental research in the field of EUV lithography for various semiconductor applications, including measuring phase of EUV masks for lithographic imaging[CI2] and investigating next-generation designs for EUV photomasks.[CI3]

2.6.1 Recent Achievements

A. Learned Adaptive Multiphoton Illumination Microscopy

Practical imaging systems, from miniature microscopes to large-scale space telescopes, are all subject to imperfections that are infeasible—and in some cases impossible—to fix with optical design and engineering. In particular, spatially-varying blur, is difficult to correct, making recovery of critical scene features a challenge. Image deblurring is an important digital method to overcome some of these imperfections. However, existing approaches are either purely analytical methods (robust but slow and calibration-heavy), or purely phenomenological methods using deep learning (fast and accurate but require large datasets).

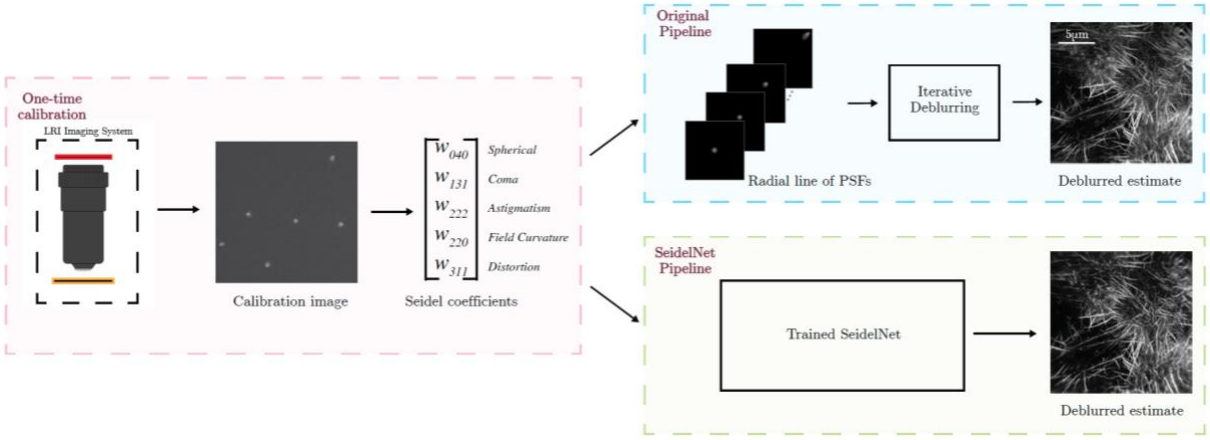

Figure 16. Comparing the two linear revolution-invariant (LRI) deblurring pipelines. The original, pictured in blue, requires an additional step of generating a stack of PSFs. The SeidelNet pipeline, on the other hand, can directly utilize the Seidel Coefficients.

To address this challenge, the **Waller** group recently introduced SeidelNet, a general-purpose deep-learning hybrid strategy for spatially-varying deblurring which learns to invert an imaging system's blurring process from a single calibration image.[CI4] This method incorporates the five primary Seidel aberration coefficients in order to perform fast, accurate, and robust deblurring with only a single calibration image per imaging system (Figure 16). The key idea behind our hybrid model is that most imaging systems are rotationally symmetric, which means their system aberrations can be parameterized with the Seidel polynomial. The method learns the five primary coefficients of the Seidel polynomial from a single image of a few randomly scattered point sources and uses them to obtain a system-specific, aberration-aware deblurring neural network. The team trained and tested SeidelNet on synthetically blurred images from the CARE fluorescence microscopy dataset, and found that, despite relatively few parameters, SeidelNet outperforms both analytical methods as well as a standard deblurring neural network.

B. Optimized Control of Adaptive X-Ray Optics

In past work, the **Waller** group developed metrology methods for significantly improving deep UV microcopy without requiring hardware modifications or the fabrication of test objects. For example, the group used this approach, which is suitable for any full-field imaging system that has coherent, steerable illumination, to successfully characterize the aberrations of the SHARP High-NA Actinic Reticle Review Project (an EUV microscope that operates near 13.5 nm wavelength).[CI5] In this period, the **Waller** group reported a data-driven modeling and control method to improve performance of adaptive X-ray mirrors, which are used on high-coherent-flux synchrotron and X-ray free-electron laser beamlines where dynamic phase control and aberration compensation are necessary.[CI6] The team demonstrated that the combination of a data-driven model for piezo-bimorph adaptive mirror shape dynamics and an optimization-based control strategy was able to reduce residual mirror figure errors in open-loop operation below 2 nm RMS, outperforming linear models and achieving the shape control accuracy required to achieve diffraction-limited performance in the X-ray regime. This new method effectively accounts for creep and hysteresis, nonlinear properties that currently limit the performance of such devices in open-loop operation (Figure 17). Accurate predictive modeling to achieve stable arbitrary surface

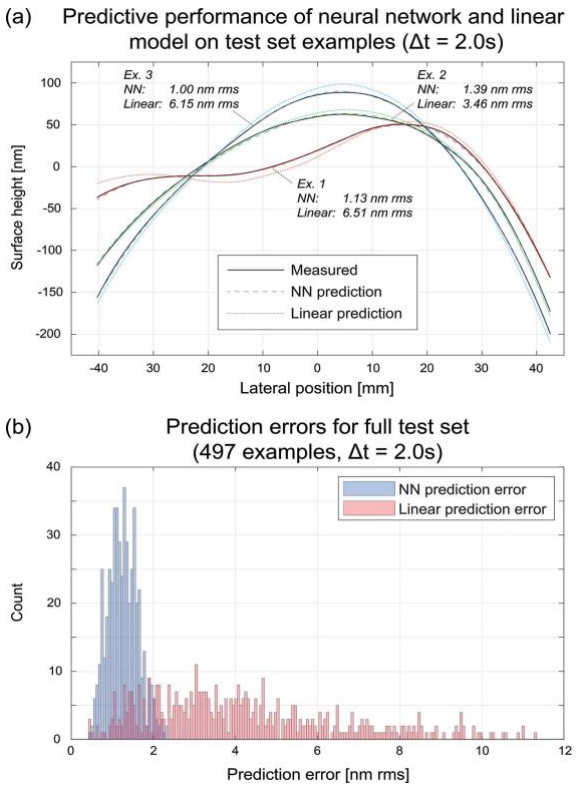

Figure 17. Performance of predictive model on test data. **(a)** Predicted curves from the neural network and linear models for three dataset examples. **(b)** Predictive performance of neural network and linear models across a full test dataset.

shapes is essential for effective deployment on high-coherent-flux X-ray beamlines where continuous feedback may be difficult to implement. An important feature of this new calibration method is that it is simple to implement and easily automated, requiring only a sequence of random shape.

C. Fourier Ptychographic Microscopy

Fourier ptychographic microscopy is a powerful computational imaging technique. It can provide quantitative phase information and high resolution over a large field-of-view, presenting numerous advantages over conventional microscopy. However, model mismatch due to unknown optical aberrations can significantly limit the reconstruction quality. A practical way of correcting for aberrations without additional data capture is through the algorithmic self-calibration embedded pupil recovery (EPRY) method, in which a pupil recovery step is embedded into the reconstruction algorithm. A severe drawback of this software-only aberration correction method is its limited accuracy.

Addressing this limitation, the **Waller** group developed a new approach, implementing a simple, dedicated calibration procedure for applications requiring high accuracy.[CI7] In simulations, they found that for a target sample reconstruction error, imaging without any aberration corrections can be done only up to a maximum aberration magnitude of λ/40. When using algorithmic self-calibration, an aberration magnitude up to λ/10 can be tolerated, whereas with the newly proposed diffuser calibration technique, this working range can be extended to λ/3. The team demonstrated that diffuser-based aberration recovery is a more robust method, even when shot noise is introduced into the system (Figure 18). Additionally, imaging systems with a large field-of-view often suffer from field-varying aberrations, which can severely degrade Fourier ptychographic microscopy reconstructions unless properly compensated. By extending correctable aberration magnitudes, diffuser calibration can extend the usable field-of-view since field-varying aberrations tend to become stronger with increased off-axis distance. Given that EUV photomask blanks generally satisfy the weak-phase roughness required for diffuser-based

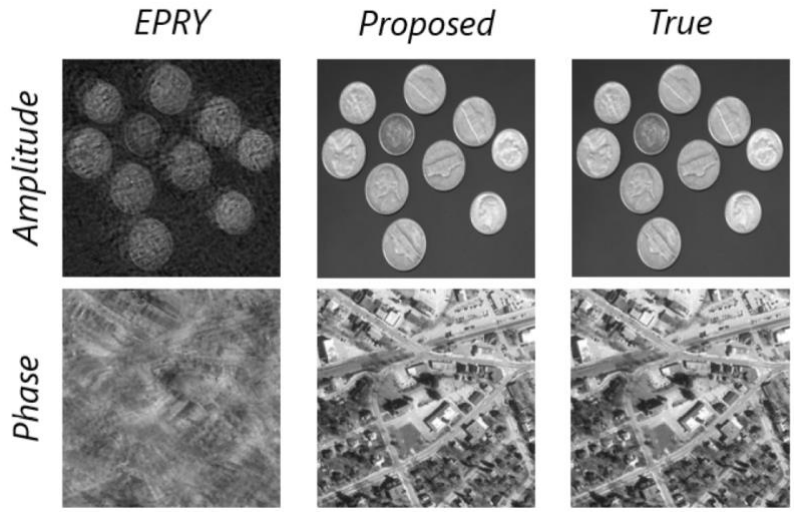

Figure 18. Results of Fourier ptychographic microscopy (FPM) reconstruction quality in an aberrated system (λ/5 waves-rms of wavefront error) with two types of calibration: purely computational calibration (EPRY) and the proposed diffuser calibration step (Proposed). Whereas EPRY suffers from significant artifacts such as crosstalk between phase and amplitude, as well as low-frequency phase errors, the proposed calibration achieves a much more faithful reconstruction for both pupil and object, with minimal reconstruction artifacts.

aberration recovery, the new correction technique by the **Waller** group is a competitive and straightforward method for EUV phase imaging systems with aberrations.

2.6.2 Current Projects

Computational Microscopy for EUV Applications

(Prof. Laura Waller)

The Waller group is working on computational microscopy techniques applied to EUV and optical metrology. For example, they can use custom partially coherent illumination patterning and computational inverse problems, or phase masks in the pupil plane, to accurately recover the wavefront phase delays to a fraction of a wavelength, thus giving morphological measurements for masks and potentially wafer-level features. These methods offer resolution well beyond the diffraction limit imposed by the imaging system's numerical aperture, along with a large field-of-view for large-scale metrology applications.

2.6.3 Publications (Computational Imaging – CI)

CI1. L. Waller, "Computational Phase Microscopy," *Proc. SPIE, Biophotonics and Biomedical Microscopy*, vol. 11575, pp. 1157502, Oct 2020.

CI2. S. Sherwin, R. Miyakawa, M. Benk, L. Waller, A. Neureuther, and P. Naulleau, "Measuring EUV Mask 3D Effects with Hyperspectral Zernike Phase Contrast," *Proc. SPIE, Extreme Ultraviolet (EUV) Lithography XII*, vol. 11609, pp. 116090B, Mar 2021.

CI3. S. Sherwin, L. Waller, A. Neureuther, and P. Naulleau, "Advanced Multilayer Mirror Design to Mitigate EUV Shadowing," *Proc. SPIE, Extreme Ultraviolet (EUV) Lithography X*, vol. 10957, pp. 1095715, Mar 2019.

CI4. E. Whang, D. McAllister, A. Reddy, A. Kohli, and L. Waller, "SeidelNet: an aberration-informed deep learning model for spatially varying deblurring," *Proc. SPIE 12438, AI and Optical Data Sciences IV*, paper 124380Y, Mar 2023.

CI5. G. Gunjala, A. Wojdyla, S. Sherwin, A. Shanker, M. P. Benk, K. A. Goldberg, P. P. Naulleau, and L. Waller, "Extreme ultraviolet microscope characterization using photomask surface roughness," *Scientific Reports*, vol. 10, pp. 11673, Jul 2020.

CI6. G. Gunjala, A. Wojdyla, K. A. Goldberg, Z. Qiao, X. Shi, L. Assoufid, and L. Waller, "Data-driven modeling and control of an X-ray bimorph adaptive mirror," *J. Synchrotron Rad.*, vol. 30, pp. 57-64, Jan 2023.

CI7. E. Li, S. Sherwin, G. Gunjala, and L. Waller, "Exceeding the limits of algorithmic self-calibrated aberration recovery in Fourier ptychography," *Opt. Continuum*, vol. 2, pp. 119-130, Jan 2023.

2.7 Optical Interconnects and Integration

Silicon photonics technology is rapidly being adopted for high-speed communication between servers within data centers because optical signals can propagate faster and with better energy efficiency than voltage signals. Light also can be used to transmit data across a chip, through silicon microstructures which act as waveguides. However, significant improvements in various optical components (including the efficiency of miniature light emitters, sensitivity of photodetectors, speed of optical switches, efficiency of waveguide couplers, etc.) are needed for optical interconnects and systems to overtake electrical interconnects. For example, in terms of energy-efficiency, the current state-of-the-art is hundreds of fJ/bit, which is orders of magnitude greater than the quantum limit of 20 aJ/bit. BETR Center researchers from the groups of **Professors Ali Javey**, **Vladimir Stojanović**, **Ming Wu**, and **Eli Yablonovitch** are addressing these needs by investigating new lights sources such as optical antenna-enhanced LEDs, and by exploring novel approaches to alleviate tradeoffs between photodetector speed, capacitance, and optical absorption, by researching new materials for optoelectronic components, and by revolutionizing random-access optical beam steering systems.[OI1-OI5]

2.7.1 Recent Achievements

A. Novel Optoelectronics with Black Phosphorus

Recently, the **Javey** group discovered black phosphorus as an excellent candidate for high-performance room-temperature infrared optoelectronics with actively variable spectra. Using the highly strain-sensitive nature of the bandgap of black phosphorus (0.22-0.53 eV), the team demonstrated a continuous and reversible tuning of the operating wavelengths in black phosphorus–MoS_2 light-emitting diodes and photodetectors.[OI5] In this period, the **Javey** group found an unusual behavior of black phosphorus by studying the thickness dependence of its photoluminescence quantum yield at room temperature.[OI6]

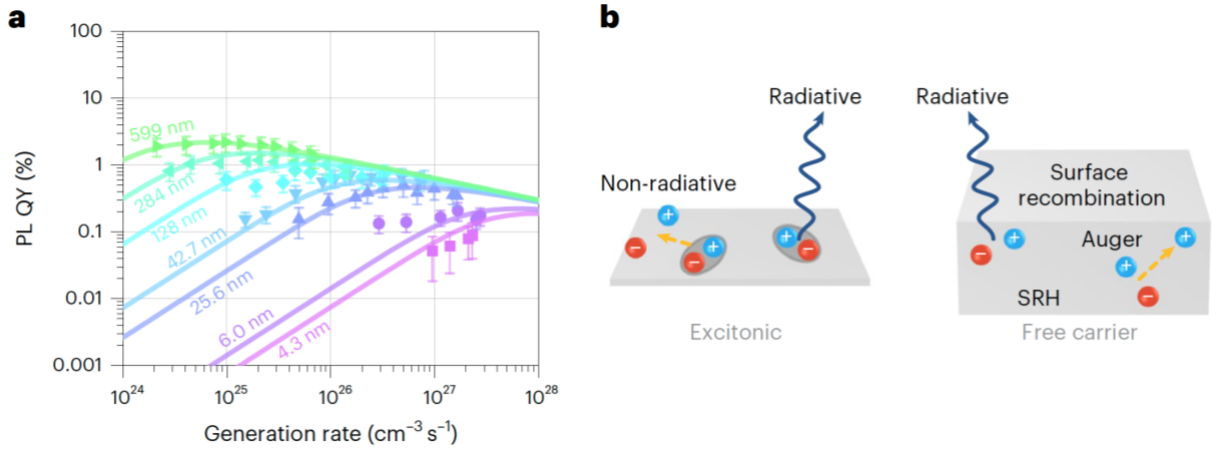

Figure 19. a) Free-carrier recombination in black phosphorus. **a.** Experimental (scatters) and calculated (solid lines) photoluminescence quantum yield (PL QY) versus generation rate for black phosphorus of different thicknesses. **b.** Dominant recombination pathways active in black phosphorus with excitonic and free-carrier systems.

By monitoring the various radiative and non-radiative recombination rates in black phosphorus as the thickness decreased from bulk to ~4 nm, the team initially discovered a drop in the photoluminescence quantum yield due to enhanced surface carrier recombination. However, this was followed by an unexpectedly sharp increase in photoluminescence quantum yield with further thickness scaling, reaching an average value of ~30% for black phosphorus monolayers (i.e., phosphorene). They found that this trend arises from the free-carrier-to-excitonic transition in black phosphorus thin films, and differs from the behavior of conventional semiconductors, where photoluminescence quantum yield monotonically deteriorates with decreasing thickness (Figure 19). Furthermore, they reported that the surface carrier recombination velocity of black phosphorus is two orders of magnitude lower than the lowest value reported in the literature for any semiconductor with or without passivation; this is due to the presence of self-terminated surface bonds in black phosphorus.

B. Center Feature Fusion Technique for LIDAR Applications

In the previous period, the **Wu** group reported a breakthrough two-dimensional random-access optical beam steering system for applications in light detection and ranging (LiDAR) and free-space optical communications. This new optical beam steering system with a record 128×128-element two-dimensional silicon photonics focal plane with random-access 2D beam steering, featuring a 70°×70° field-of-view with a 0.6°×0.6° resolution, a beam divergence of 0.050°×0.049°, and sub-MHz steering speed.[OI4] In this period, the team addressed a different challenge for building accurate and robust 3D object detection systems: the leverage of multi-modal fusion between camera and LiDAR. Current approaches include the point decorating method, in which point clouds are augmented with camera features. However, this method fails to utilize the higher resolution images from cameras. Alternatively, projecting camera features to the bird's-eye-view (BEV) space for fusion have been proposed, however they require projecting millions of pixels, most of which only contain background information.

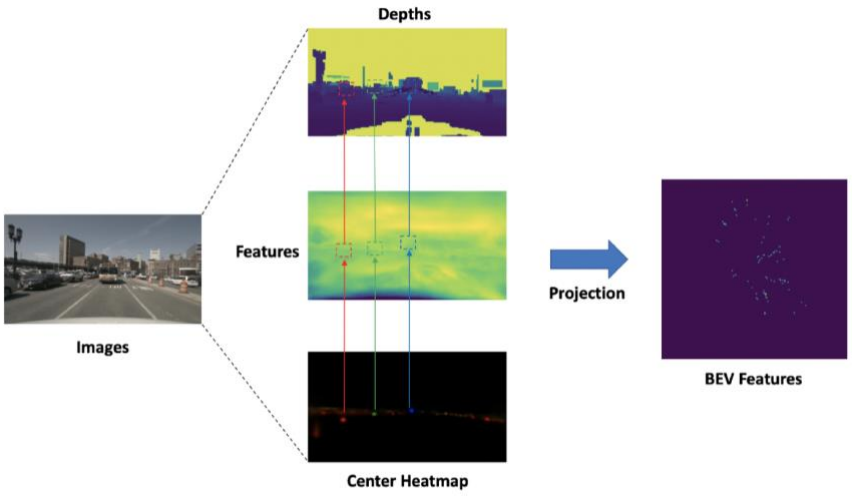

Figure 20. Proposed selective feature projection. The detection heatmap is used to select interesting regions from the corresponding deep feature map. Dense depth predictions are then used to project the corresponding features to BEV, where they can be fused with LiDAR BEV features.

In response, the **Wu** group proposed the Center Feature Fusion (CFF) technique, in which center-based detection networks are leveraged in both the camera and LiDAR streams to identify relevant object locations.[OI7] While also

leveraging the power of the BEV representation, instead of projecting all the camera features into BEV, which is wasteful since most pixels simply represent background, the CFF technique uses center-based detection to identify the locations of pixel features relevant to object locations (Figure 20). This is typically only a small fraction of the total number in the image and are then projected and fused in the BEV frame. On the nuScenes dataset, this new method outperformed the LiDAR-only baseline by 4.9% mAP while fusing up to 100x fewer features than other fusion methods.

C. High-Efficiency Metal-Dielectric Optical Antennas

Low power silicon based light source and detector are attractive for on-chip photonic circuits given their ease of process integration. However, conventional silicon light emitting diodes emit photons with energies near the band edge where the corresponding silicon photodetectors lack responsivity. On the other hand, previously reported hot carrier electroluminescent silicon devices utilizing a reverse biased diode require high operating voltages. To solve this discrepancy, the **Javey** group investigated hot carrier electroluminescence in silicon metal–oxide–semiconductor capacitors operating under transient voltage conditions.[OI8]

The team found that during each voltage transient, large energy band bending is created at the edge of the source contact, much larger than what is achievable at a steady state. As a result, electrons and holes are injected efficiently from a single source contact into the silicon channel at the corresponding voltage transient, where they subsequently undergo impact ionization and phonon-assisted interband recombination (Figure 21). Notably, they demonstrated low voltage operation down to 2.8 V by using a 20 nm thick high-*k* gate dielectric. Moreover, further voltage scaling will be possible by reducing the gate dielectric thickness, thus presenting a low voltage platform for silicon optoelectronic integrated circuits.

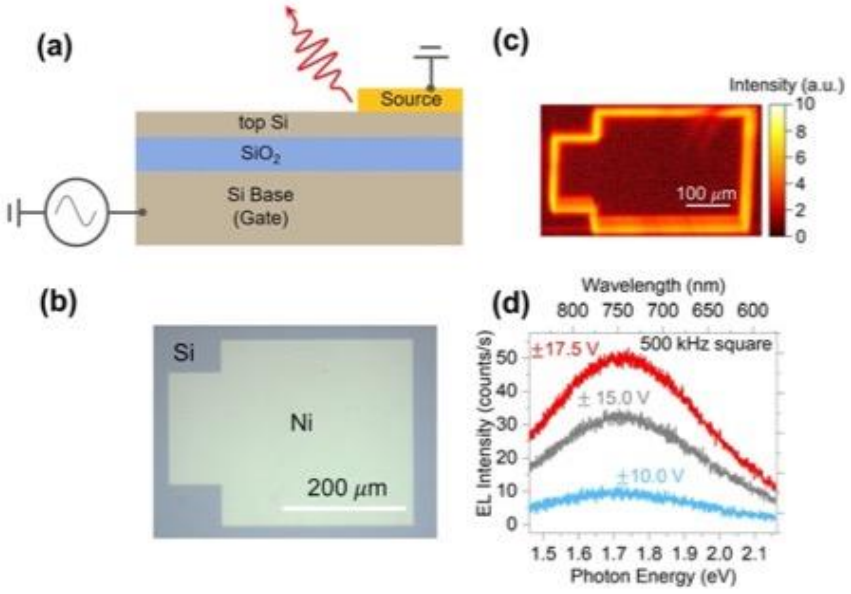

Figure 21. Transient electroluminescence in silicon. (**a**) Schematic cross section of the device. (**b**) Optical micrograph. (**c**) EL image of the device portraying luminescence along the periphery of Schottky junction under ac excitation. (**d**) EL spectra at various gate voltages for a silicon-on-insulator device having top silicon thickness of 12 nm and buried oxide 25 nm.

2.7.2 Current Projects

Silicon Photonic Super-Switch

(Prof. Ming Wu)

The goal of this project is to develop large-scale silicon photonic switches (1000x1000) with fast response time (microsecond) and low optical loss (3dB fiber-to-fiber). This project has 3 tasks: Task 1 will develop scalable silicon photonic MEMS technology with super low loss. Task 2 will develop custom CMOS ASICs that will be directly flip-chip integrated on Si photonic switch for digital control. Task 3 will develop array fiber packaging technology with low insertion loss (< 0.5 dB). The team is currently in Phase 1 whose goal is to demonstrate 128x128 silicon photonic switch with integrated CMOS control and 8 dB fiber-to-fiber loss.

Efficient LEDs Based on Defect-Tolerant Materials

(Prof. Ali Javey)

Previously, the Javey group observed that for transition metal dichalcogenide (TMDC) monolayer semiconductors (e.g., MoS2, WS2, WSe2) there was a sharp drop in photoluminescence quantum yield (PLQY) at high exciton concentrations due to exciton-exciton annihilation (EEA), which is non-radiative. This was a major limitation for the use of monolayers in efficient practical devices. Recently (unpublished), they showed that EEA is resonantly amplified in TMDC monolayers by van Hove singularities (VHSs) present in their joint density of states. Logarithmic VHSs are a hallmark of two-dimensional semiconductors. By applying small mechanical strain (~0.2%), the EEA process is shifted away from the VHS resonance and circumvent the enhanced nonradiative EEA that plagues the PLQY at high exciton densities, leading to near-unity PLQY at all exciton densities in 2D TMDC monolayers. Combined with counterdoping, this simple method suppresses all nonradiative recombination at all generation rates for both exfoliated and CVD-grown centimeter-scale TMDC monolayers. The group has studied materials physics and is now ready to build devices to prove the concept.

Compact Fourier Transform Infrared Spectrometer on Chip

(Prof. Ming Wu)

The goal of this project is to investigate and prototype chip-scale Fourier-Transform Infrared (FTIR) spectrometer enabled by low-loss silicon photonic micro-electro-mechanical-system (MEMS) switches and on-chip delay lines.

Variable Spectrum Optoelectronics

(Prof. Ali Javey)

Some 2D semiconductors exhibit a large band structure modulation by strain, larger than what is seen in classical systems. Furthermore, they can inherently tolerate larger strain values due to crystal structure. Taking advantage of these features, the Javey group has recently built actively variable spectrum LEDs and photodetectors for which a single device shows wavelength tunability from ~0.2 to 0.5 eV by applying a mechanical strain. It's effectively a MEMs device and by tuning the strain, the emission or absorption peak can be actively tuned from LWIR to mid-IR

(unpublished, recently submitted). The group is exploring opportunities for various applications including spectroscopy.

Photonically-Remoted Endoscopic Ultrasound Array

(Prof. Vladimir Stojanović)

The Stojanović group is developing an ultrasound array readout beamforming system that consists of the low-power ring-resonator ultrasound sensor array chip (with thousands of sensors in an ultrasound probe integrated with ring thermal tuners) with a companion remoted receiver array chip. The ultrasound sensing capability of the ring resonator array opens the new applications beyond endoscopic ultrasound, such as photoacoustic imaging.

2.7.3 Publications (Optical Interconnects – OI)

OI1. S. A. Fortuna, A. Taghizadeh, E. Yablonovitch, and M. C. Wu, "Toward 100 GHz Direct Modulation Rate of Antenna Coupled NanoLED," *IEEE Photonics Conference*, Jan 2016.

OI2. K. Settaluri, C. Lalau-Keraly, E. Yablonovitch, and V. Stojanović, "First Principles Optimization of Opto-Electronic Communication Links," IEEE Transactions on Circuits and Systems I: Regular Papers , vol.64, no.5, pp. 1270-1283, May 2017.

OI3. D.-H. Lien, M. Amani, S.B. Desai, G.H. Ahn, K. Han, J.-H. He, J.W. Ager, M.C. Wu, and A. Javey, "Large-Area and Bright Pulsed Electroluminescence in Monolayer Semiconductors," *Nature Communications*, vol. 9, pp. 1229, Mar 2018.

OI4. X. Zhang, K. Kwon, J. Henriksson, J. Luo, and M. C. Wu, "A large-scale microelectromechanical-systems-based silicon photonics LiDAR," *Nature*, vol. 603, pp. 253-258, Mar 2022.

OI5. H. Kim, S. Z. Uddin, D.-H. Lien, M. Yeh, N. S. Azar, S. Balendhran, T. Kim, N. Gupta, Y. Rho, C. P. Grigoropoulos, K. B. Crozier, and A. Javey, "Actively Variable-Spectrum Optoelectronics with Black Phosphorus," *Nature*, vol. 596, pp. 232-237, Aug 2021.

OI6. N. Higashitarumizu, S. Z. Uddin, D. Weinberg, N. S. Azar, I. K. M. R. Rahman, V. Wang, K. B. Crozier, E. Rabani, and A. Javey, "Anomalous thickness dependence of photoluminescence quantum yield in black phosphorous," *Nature Nanotechnol.*, Online Published, Mar 2023.

OI7. P. Jacobson, Y. Zhou, W. Zhan, M. Tomizuka, and M. C. Wu, "Center Feature Fusion: Selective Multi-Sensor Fusion of Center-based Objects," *arXiv: 2209.12880*, Sep 2022.

OI8. I. K. M. R. Rahman, S. Z. Uddin, H. Kim, N. Higashitarumizu, and A. Javey, "Low voltage AC electroluminescence in silicon MOS capacitors," *Appl. Phys. Lett.*, vol. 121, pp. 193502, Nov 2022.

3. Knowledge Transfer

3.1 Overview

Knowledge transfer is at the heart of the BETR Center's mission of fostering groundbreaking discoveries and fertilizing new technologies. In the BETR Center, knowledge transfer is seen as a two-way street: Sharing the latest research outcomes of BETR with various stakeholders, while bringing new knowledge into the Center by engaging with its industry affiliate members and other key players in semiconductor technologies.

In fact, the BETR Center was established with the recognition that partnerships with leading semiconductor companies are a key factor in accelerating research, education and outreach endeavors. Since then, the Center has put significant efforts into sharing new knowledge with industry, academia and research labs. Interactions have taken place at various levels, including seminars/webinars by internal and external speakers, visits and customized briefings (online or in-person) for BETR Center industry affiliates, and biannual BETR Center workshops.

Additional knowledge transfer vehicles used by the BETR Center for sharing new discoveries with the wider research community are publications in scientific journals and conferences proceedings, as well as patents and invention disclosures. To that end, the BETR Center shares a list of research publications (including copies of published papers) and patent applications with all industry affiliates as part of the annual report and on the BETR Center website (https://betr.berkeley.edu/). Moreover, if requested by an industry affiliate, technology licensing will be facilitated by introductions to the UC Berkeley Industry Alliances Office and the Office of Technology Licensing.

Finally, the BETR Center recognizes that education itself is an important knowledge transfer element by preparing the Center's students and postdoctoral researchers to be the next-generation leaders in physical electronics and semiconductor technologies. The BETR Center facilitates interaction of Center students and postdocs with representatives of its industry affiliates through seminars/webinars, poster sessions at the biannual BETR Center Workshops, and targeted recruiting events (upon request by industry affiliates). Furthermore, the Center has been working with industry affiliates in identifying BETR Center students and postdocs for internship positions.

In the following, detailed information about activities in the last year in BETR Center's four main knowledge transfer areas are provided:

- BETR Center Workshops
- Solid State Technology and Devices Seminars/Webinars
- Publications in Scientific Journals and Conference Proceedings
- Intellectual Property and Invention Disclosures

3.2 BETR Center Workshops

The workshops of the BETR Center, held twice annually, are prime knowledge transfer opportunities, connecting faculty, postdocs and students of the Center with representatives of its industry affiliates and other invited companies from the semiconductor industry. After two years of restricting BETR Center Workshops to online-only events due to COVID-19 restrictions, we were pleased to hold both workshops in 2022 in the traditional in-person/on-campus form. Workshops feature oral presentations from BETR Center researchers, lightning talks and a poster session by the Center's students and postdocs, as well as industry panels and broad discussion forums about the latest technology trends and challenges. In addition, all workshops include a one-hour closed session between the BETR Center leadership and members of the Technical Advisory Board (with representatives from all industry affiliates).

All workshop presentations are recorded and made available to industry affiliates on the BETR Center website (https://betr.berkeley.edu/). Note that a BETR Center website account (with unique username/password) is needed to access the recordings. BETR Center website accounts may be requested by representatives of industry affiliates by email to betr@berkeley.edu.

Spring 2022 Workshop

The Spring 2022 Workshop of the BETR Center as an in-person event on the UC Berkeley campus on May 31, 2021. In addition, an online event on May 26, featuring lightning talks by BETR Center students and postdocs, preceded the in-person event (see Appendix B and Appendix C for the agendas of the in-person and online events, respectively). The in-person workshop was attended by 54 participants, including 22 BETR Center students and postdocs and 19 representatives from industry. In addition, 23 representatives from industry also registered for the online Student & Postdoc Lightning Talks event. The in-person event featured seven talks by BETR Center co-directors and postdocs, and 13 student/postdoc poster presentations.

Representatives of the following BETR Center industry affiliates participated in the closed session meeting of the Technical Advisory Board with BETR Center Leadership: **Applied Materials**, **Lam Research**, **TSMC**, **Intel Corporation,** and **Meta** (Facebook).

Talks by BETR Center co-Directors and Postdocs

- **Ali Javey:** "Room-temperature Deposited Tellurium Thin Films for p-type Field-effect Transistors, Circuits, and Photodetectors"
- **Sayeef Salahuddin:** "Ultra-low EOT Gate Oxide Using Ferroelectric HfO2-ZrO2 Superlattice"
- **Ramamoorthy Ramesh:** "Voltage and Current Controlled Nanomagnetism for Memory and Logic"
- **Jeffrey Bokor:** "Progress Towards Picosecond On-chip Magnetic Memory"

- **Vladimir Stojanovic:** “Electronic-Photonic Systems-on-Chip”
- **Johannes Henriksson:** “Large-scale Silicon Photonic MEMS Switches”
- **Laura Waller:** “Computational Microscopy”

Lightning Talks and Posters by BETR Center Students and Postdocs

- **Ruocheng Wang** (Stojanović group), “Electronic-Photonic System for Massive-MIMO mm-wave Applications”
- **Xiaoxi Huang** (Ramesh group), “Non-volatile Ferroelectrically Controlled Spin Transport in Multiferroic $BiFeO_3$ at Room Temperature”
- **Suraj Cheema** (Salahuddin group), “Physical Limits of Ferroelectricity and Negative Capacitance for Equivalent Oxide Thickness Scaling”
- **Nirmaan Shanker** (Salahuddin group), “Reliability and Ultrafast Characterization of Negative Capacitance HfO_2-ZrO_2 Gate Stack”
- **Naoki Higashitarumizu** (Javey group), “Dynamic Spectrum Optoelectronics with Black Phosphorus”
- **Lars Tatum** (Liu group), “Semiconductor Negative Differential Resistance (NDR) Device for Compact Integrated Circuits”
- **Sucheta Mondal** (Bokor group), “Optically Switchable Nanoscale Magnetic Tunnel Junction”
- **Hanuman Singh** (Bokor group), “Effect of Ultrafast Laser Heating on Electrical Switching of LCO Devices”
- **Daniel Klawson** (Wu group), “Integrated Optical MEMS for Scalable Trapped Ion Quantum Computing”
- **Isaac Harris** (Ramesh group), “The Spin Hall Effect in Epitaxial Oxide Heterostructures of BPBO and LSMO”
- **Tsegereda Esatu** (Liu group), “Nanoscale Contact Welding for Programmable Relays”
- **Maykel Nijenhuis** (Arias group), “Tin Perovskites with 2D/3D Structure”
- **Li-Chen Wang** (Salahuddin group), “Demonstration of Low EOT Gate Stack and Record Transconductance on Lg=90 nm nFETs Using 1.8 nm Ferroic HfO_2-ZrO_2 Superlattice”

Fall 2022 Workshop

The Fall BETR Workshop was held as an on-campus/in-person event on November 3, 2022 (see Appendix D for the full workshop agenda). BETR Center co-directors and students gave six talks in addition to 15 student and postdoc poster presentations. In addition, the 15 students and postdocs recorded lightning talk video recordings, which were shared with all workshop attendees one week prior to the event. The Fall Workshop also featured a panel discussion on "The Role of Internships in Workforce Development: Opportunities and Challenges", moderated by BETR co-Director **Prof. Laura Waller**, with the following panelists: **Dr. Nerissa Draeger** (Lam Research), **Dr. Uygar Avci** (Intel), **Dr. Philip Kraus** (Applied Materials), **Dr. Han Wang** (TSMC), and **Dr. Yach Lai** (Cadence). The workshop was attended by 48 participants, including 22 BETR Center students and postdocs and 12 representatives from industry.

The closed session of the Technical Advisory Board with BETR Center leadership was attended by representatives of BETR Center industry affiliates **Applied Materials**, **Lam Research**, **TSMC**, **Intel Corporation**, **AMD**, and **SK Hynix**.

Talks by BETR Center co-Directors and Students

- **Sophia Shao:** "Generating Domain-Specific Systems at Scale"
- **Tsu-Jae King Liu:** "Simulation-Based Comparison of iFinFET and Nanosheet FET 3nm-Node Transistor Designs"
- **Ana Arias:** "Printed Flexible Electronic Systems"
- **Savaan Patel:** "Hardware-Accelerated Boltzmann Machines for Intractable Problems"
- **Ming Wu:** "Silicon Photonics for Optical Switching, 3D Sensing, and Quantum Computing"
- **Eli Yablonovitch:** "Onsager Computing – Optimization by the Principle of Minimum Heat Generation"

Lightning Talks and Posters by BETR Center Students and Postdocs

- **Sarika Madhvapathy** (Stojanović group), "Electronic-Photonic Ultrasound Receiver Array for Endoscopic Applications"
- **Jasmine Jan** (Arias group), "Flexible Blade-Coated Optoelectronic Devices: Dual Functionality via Simultaneous Deposition"
- **Vivian Wang** (Javey group), "Highly Multicolored Light-Emitting Arrays for Spectroscopy"
- **Pratik Brahma** (Salahuddin group), "Emergence of Fractional Phases due to Confinement using Convolutional Restricted Boltzmann Machines"

- **Lars Tatum** (Liu group), "Formation of Inserted-Oxide Silicon Fins for Improved FinFET Scalability"
- **I K M Reaz Rahman** (Javey group), "Low Voltage Electroluminescence in Silicon MOS Capacitors"
- **Daniel Klawson** (Wu group), "Integrated Photonics for Scalable Trapped Ion Quantum Computing"
- **Sunjin Choi** (Stojanović group), "SuperFabric: Optical Interconnect for Disaggregated Systems"
- **Niharika Gupta** (Javey group), "Bright Mid-Wave Infrared Light-Emitting Diodes Based on Black Phosphorus"
- **Lucas Lahann** and **Payton Goodrich** (Arias group), "Multianalyte Sensor Array for Measuring Agricultural Nitrogen Species"
- **Philip Jacobson** (Wu group), "Multi-Sensor Fusion of Center-Based Objects for 3D Detection"
- **Rafaela Brinn** (Ramesh group), "Coherent Electric Field Manipulation of Single-Spins in Er^{3+}-Doped $PbTiO_3$ Thin Films"
- **Maykel Nijenhuis** (Arias group), "Ion-Selective Organic Electrochemical Transistors for Bio-Sensing"
- **Noelle Davis** (Javey group), "Robust, Multimodal Sweat Sensors with High-Throughput Fabrication"
- **Jianheng Luo** (Wu group), "Integrated Microlens Coupler for Photonic Integrated Circuits"

Panel Discussion: "The Role of Internships in Workforce Development"

- **Laura Waller**, UC Berkeley (Moderator)
- **Nerissa Draeger**, Lam Research (Panelist)
- **Uygar Avci**, Intel (Panelist)
- **Philip Kraus**, Applied Materials (Panelist)
- **Han Wang**, TSMC (Panelist)
- **Yach Lai**, Cadence (Panelist)

3.3 Solid State Technology and Devices Seminar Series

The BETR Center has continued hosting the *Solid State Technology and Devices Seminar Series* of the UC Berkeley Electrical Engineering and Computer Science department. Solid State Technology and Devices seminars are usually held on Fridays (1:00-2:00 PM Pacific) by invited speakers who are experts from academia, national labs, and industry. After two years of restricting seminars to online-only events due to COVID-19 restrictions, we were pleased to hold most of the 2022/23 seminars in the traditional in-person/on-campus form with an available online simulcast. A total of 20 seminars were held in the 2022/2023 reporting period and were simulcast to BETR Center members via Webex.

Seminars are usually recorded (with permission by the speaker) and made available to industry affiliates on the BETR Center website (https://betr.berkeley.edu). Note that a BETR Center website account (with unique username/password) is needed to access the seminar recordings. BETR Center website accounts may be requested by representatives of industry affiliates by email to betr@berkeley.edu.

2022/23 Solid State Technology and Devices Seminars

- **Xiaoer Hu**, UC Berkeley, "Micro-Electro-Mechanical Relay Technology for Beyond von Neumann Architecture", May 6, 2022
- **Hagen Klauk**, Max Planck Institute for Solid State Research Stuttgart, "Flexible Nanoscale Organic Thin-Film Transistors", August 19, 2022
- **Sapan Agarwal**, Sandia National Laboratories, "Co-designing Neuromorphic Systems from Materials to Algorithms", August 22, 2022
- **Peter McMahon**, Cornell University, "Computing with Physical Systems", September 2, 2022
- **Daniel Worledge**, IBM Almaden Research Center, "Spin-Transfer-Torque MRAM: The Next Revolution in Memory", September 16, 2022
- **Supriyo Datta**, Purdue University, "Computing with p-Bits: Between a Bit and a q-Bit", September 23, 2022
- **Greg Pitner**, Taiwan Semiconductor Manufacturing Company (TSMC), "Carbon Nanotube Transistors: Recent Progress Towards Applications in Highly Scaled and High-Performance CMOS Logic", September 30, 2022
- **Keisuke Goda**, University of Tokyo, "Intelligent Image-Activated Cell Sorting", October 7, 2022

- **Sunil Bhave**, Purdue University, "Fast-Tunable and Low-Loss Stress-Optical Microsystems", October 21, 2022
- **H.-S. Philip Wong**, Stanford University, "Carbon Nanotube Transistors for a Future 3D Logic Technology", October 28, 2022
- **Jean Anne Incorvia**, The University of Texas, Austin, "Designing Artificial Synapses for Application-Specific Neuromorphic Computing Using Magnetic and 2D Materials", December 2, 2022
- **Stephen M. Wu**, Rochester University, "Strain Engineering 2D van der Waals Devices", January 27, 2023
- **Kenneth Crozier**, University of Melbourne, "Nanophotonics-Enabled Infrared Microspectrometers and Optical Tweezers", February 3, 2023
- **Youngik Sohn**, Korea Advanced Institute of Science and Technology (KAIST), "Linear Optics Quantum Computing", February 17, 2023
- **Carolin M. Sutter-Fella**, Lawrence Berkeley National Laboratory, "Mechanistic Understanding Coupled with the Discovery of Multifunctional Energy Materials", February 24, 2023
- **Carolyn R. Duran**, Intel Corporation, "Sustainability and the Future of Semiconductor Innovations", March 10, 2023
- **Erin L. Ratcliff**, University of Arizona, "Defects, Devices, and Degradation of Metal Halide Perovskites: An Electrochemist's Perspective", March 17, 2023
- **Kevin Yasumura**, Google LLC, Large Scale Optical Switching in Google Data Centers", March 24, 2023
- **Boubacar Kante**, UC Berkeley, "The Berkeley Surface Emitting Laser (BerkSEL): A Scale-Invariant Laser?", April 7, 2023
- **Maria Antonietta Loi**, University of Groningen, "Carbazole Based Self-assembly Monolayers for Highly Efficient Sn/Pb-Perovskite Solar Cells", April 14, 2023

More details about the seminars/webinars, including abstract and speaker bio, can be found in Appendix A.

3.4 Publications

1. R. Kaveh, N. Tetreault, K. Gopalan, J. Maravilla, M. Lustig, R. Muller, and A. C. Arias, "Rapid and Scalable Fabrication of Low Impedance, 3D Dry Electrodes for Physiological Sensing," *Adv. Mater. Technol.*, pp. 2200342, May 2022.
2. S. Buchbinder, R. Wang, D. Kramnik, D. Van Orden, A. Khilo, J. Fini, C. Sun, M. Wade, and V. Stojanović, "Silicon Microring Modulator for High SFDR Analog Links in Monolithic 45nm CMOS," *2022 Conference on Lasers and Electro-Optics (CLEO)*, paper SF4L.1, May 2022.
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3.5 Technology Transfer

3.5.1 Patents and Patent Applications

Int. Patent App. WO 2022 094107 A1
Spin-orbit rectifier for weak radio frequency energy harvesting
E. Yablonovitch, S. Salahuddin, S. Sayed
Application Publ. Date: May 5, 2022

US Patent App. 17/503,999
Scalable and High-Performance Pressure Sensors for Wearable Electronics
A. C. Arias, X. Wu, Y. T. Khan, J. K. Ting, N. A. D. Yamamoto
Application Publ. Date: May 12, 2022

US Patent 16/768,233
Wafer-scale-integrated silicon-photonics-based optical switching system and method of forming
T. J. Seok, M. C. A. Wu
Patent Granted Date: June 14, 2022

US Patent App. 17/691,437
Organic multi-channel optoelectronic sensors for wearable health monitoring
Y. Khan, D. Han, J. Ting, M. Ahmed, A. C. Arias
Application Publ. Date: June 23, 2022

US Patent App. 17/594,605
Gas sensors with negligible response to humidity and temperature
N. Gupta, A. Javey, H. M. Fahad
Application Publ. Date: June 30, 2022

US Patent 16/564,306
Single screen fabrication of symmetric multilayer magnetic resonance imaging (MRI) receive coils
S. M. Lustig, A. C. Arias, J. R. Corea, A. M. Flynn
Patent Granted Date: August 2, 2022

US Patent App. 17/608,355
Low band gap graphene nanoribbon electronic devices
F. R. Fischer, J. Bokor, Z. Mutlu, J. P. Llinas, R. D. Mccurdy, G. C. Veber, D. J. Koenigs
Application Publ. Date: September 8, 2022

US Patent 17/252,671
Beam-steering System Based on a MEMS-Actuated Vertical-Coupler Array
X. Zhang, M. C. A. Wu, A. S. Michaels, J. Henriksson
Patent Granted Date: September 13, 2022

US Patent App. 17/745,383
Potentiometric mechanical sensors and temperature sensors
A. C. Arias, X. Wu
Application Publ. Date: December 22, 2022

US Patent App. 17/892,622
Lithium-ion battery impending failure detection
H. M. Fahad, A. Javey
Application Publ. Date: December 8, 2022

US Patent App. 17/758,221
Multi-gas detection with cs-fet arrays for food quality assessment
Z. Yuan, M. Bariya, H. M. Fahad, R. Han, N. Gupta, A. Javey
Application Publ. Date: January 26, 2023

US Patent App. 17/399,583
Voltage-controlled gain-cell magnetic memory
S. Salahuddin, S. Sayed
Application Publ. Date: February 16, 2023

US Patent 17/153,421
Three-dimensional scanless holographic optogenetics with temporal focusing
L. Waller, H. Adesnik, N. C. Pégard
Patent Granted Date: February 28, 2023

3.5.2 Available Technologies

Tech ID: 32471
Biodegradable Potentiometric Sensor to Measure Ion Concentration in Soil
BETR Faculty: Ana Claudia Arias

Tech ID: 32359
Superlattice, Ferroic Order Thin Films for Use as High/Negative-k Dielectric
BETR Faculty: Sayeef Salahuddin

Tech ID: 32153
Spin-orbit Rectifier for Weak Radio Frequency Energy Harvesting
BETR Faculty: Eli Yablonovitch, Sayeef Salahuddin

Tech ID: 30358
Low Band Gap Graphene Nanoribbon Electronic Devices
BETR Faculty: Jeffrey Bokor, Felix Fischer

Tech ID: 30280
A potentiometric mechanical sensor
BETR Faculty: Ana Claudia Arias

Tech ID: 30190
Organic Multi-Channel Optoelectronic Sensors for Smart Wristbands
BETR Faculty: Ana Claudia Arias

Tech ID: 29987
Scalable and High-Performance Pressure Sensors for Wearable Electronics
BETR Faculty: Ana Claudia Arias

Tech ID: 29669
Pulse Oximeter Using Ambient Light
BETR Faculty: Ana Claudia Arias

Tech ID: 29091
Printed All-Organic Reflectance Oximeter Array
BETR Faculty: Ana Claudia Arias

Tech ID: 27270
Simultaneous Doctor Blading of Different Colored Organic Light Emitting Diodes
BETR Faculty: Ana Claudia Arias

Tech ID: 25799
Optical Phase Retrieval Systems Using Color-Multiplexed Illumination
BETR Faculty: Laura Waller

Tech ID: 25573
Enhancing Photoluminescence Quantum Yield for High Performance Optoelectrics
BETR Faculty: Ali Javey

Tech ID: 25105
Compressive Plenoptic Imaging
BETR Faculty: Laura Waller

Tech ID: 24717
Enhanced Patterning of Integrated Circuits
BETR Faculty: Tsu-Jae King Liu

Tech ID: 24184
Chemical-Sensitive Field-Effect Transistor
BETR Faculty: Ali Javey

Tech ID: 23976
Partially Coherent Phase Recovery by Kalman Filtering
BETR Faculty: Laura Waller

Tech ID: 23955
A Thin Film VLS Semiconductor Growth Process
BETR Faculty: Ali Javey

Tech ID: 23488
Printed Organic LEDs And Photodetector for A Flexible Reflectance Measurement-Based Blood Oximeter
BETR Faculty: Ana Claudia Arias

Tech ID: 23092
Micro Electromechanical Switch Design with Self Aligning and Sub-Lithographic Properties
BETR Faculty: Tsu-Jae King Liu

Tech ID: 18962
Improved Mechanical Contact Reliability and Energy Efficiency for CMOS Applications
BETR Faculty: Tsu-Jae King Liu

Tech ID: 18103
Nanowire-based Chemical Connector for Miniature-Scale Applications
BETR Faculty: Ali Javey

Tech ID: 17830

Low Cost, Low-Temperature Polycrystalline Semiconductor Films for Solar Cells and Large Scale Integrated Circuits

BETR Faculty: Tsu-Jae King Liu

Tech ID: 17370

Low Voltage Mems Flash Memory

BETR Faculty: Tsu-Jae King Liu

Tech ID: 17319

Platform for Batch Integration of Dissociated or Incompatible Technologies

BETR Faculty: Tsu-Jae King Liu

4 Appendices

BETR Solid State Technology and Devices Seminar

Friday, May 6, 2022

Micro-Electro-Mechanical Relay Technology for Beyond Von Neumann Architecture

Xiaoer Hu
Graduate Student, Liu Group
Electrical Engineering and Computer Science
UC Berkeley

Abstract: Micro-electro-mechanical (MEM) relays previously have been shown to be promising for energy-efficient digital computing applications, due to their abrupt ON/OFF switching characteristics and negligible off-state leakage current. In this talk, novel applications of MEM relays will be presented. First, we will demonstrate that MEM relays can operate reliably with millivolt signals at cryogenic temperatures, due to much lower hysteresis voltage and more stable ON-state resistance. A sub-10 mV relay-based inverter circuit is demonstrated at a temperature of 4 K. Our experimental study indicates that MEM relays should be able to operate at temperatures as low as 1.8 K, making them promising candidates for ultra-low power cryogenic digital interface circuits for quantum computing. Second, the DC-bias-dependent oscillatory behavior of MEM relays is investigated via experimental study and finite-element-method-based computer simulations. Sub-harmonic injection locking and coupled oscillation behaviors of MEM relays are demonstrated, indicating that MEM relay oscillators are promising for implementing Ising machines, which can solve combinatorial optimization problems much more efficiently than conventional computer architectures.

Bio: Xiaoer Hu is a Ph.D. candidate in Professor Tsu-Jae King Liu's group. Her research is focused on novel applications of micro-electro-mechanical relays. She received her bachelor's degree in Materials Science and Engineering from the University of Michigan, Ann Arbor in 2017, and a bachelor's degree in Electrical and Computer Engineering from Shanghai Jiao Tong University in 2017.

BETR Solid State Technology and Devices Seminar

Friday, August 19, 2022

Flexible Nanoscale Organic Thin-Film Transistors

Hagen Klauk

Head of the Organic Electronics Group
Max Planck Institute for Solid State Research
Stuttgart, Germany

Abstract: Organic thin-film transistors (TFTs) can often be fabricated at temperatures around or below 100 degrees Celsius and thus on a wide range of unconventional substrates, including flexible and transparent polymers, such as polyethylene naphthalate (PEN). This makes organic TFTs a potential alternative to TFTs based on inorganic semiconductors, such as low-temperature polycrystalline silicon (LTPS) and indium gallium zinc oxide (IGZO), which typically require higher process temperatures that limit the choice of flexible substrate materials to ultrathin glass and polyimide. For circuit and display applications, an important TFT parameter is the transit frequency, which is the highest frequency at which transistors are able to switch or amplify electrical signals. A field-effect transistor's transit frequency depends critically on the channel length and the parasitic gate-to-source and gate-to-drain overlaps. Most of the highest transit frequencies reported for organic TFTs to date have been achieved with channel lengths and gate-to-contact overlaps of around 1 µm. To explore the static and dynamic performance of flexible organic TFTs with nanoscale dimensions, we have used electron-beam lithography and fabricated low-voltage organic TFTs with channel lengths and gate-to-contact overlaps as small as 100 nm on flexible PEN substrates. These TFTs display useful static and dynamic characteristics, including on/off current ratios of nine orders of magnitude, subthreshold swings below 100 mV/decade, turn-on voltages of 0 V, negligibly small threshold-voltage roll-off, contact resistances below 1 kOhm-cm, and switching delays below 20 ns.

Bio: Dr. Hagen Klauk received his Ph.D. degree in electrical engineering from Pennsylvania State University in 1999. From 1999 to 2000, he was a Postdoctoral Researcher at Penn State. In 2000, he joined Infineon Technologies, Erlangen, Germany. Since 2005, he has been Head of the Organic Electronics Group at the Max Planck Institute for Solid State Research, Stuttgart, Germany. His research focuses on organic thin-film transistors.

BETR Solid State Technology and Devices Seminar

Monday, August 22, 2022

Co-designing Neuromorphic Systems from Materials to Algorithms

Sapan Agarwal

Principal Member of Technical Staff
Sandia National Laboratories

Abstract: Deploying trusted artificial intelligence at the point-of-sensing or at the edge in our nation's mobile, airborne and satellite systems would enable revolutionary capabilities including persistent and ubiquitous monitoring for emerging threats, enhanced climate monitoring, and autonomous vehicles. To accomplish this, intelligent algorithms need to be co-designed with tailored analog in-memory computing to achieve 100X more compute (performance/watt) than possible with state-of-the-art technology in size, weight and power constrained extreme environments. This talk will give an overview of Sandia's work towards co-designing the entire information processing chain from materials and devices to systems, architectures, and algorithms to accelerate neural network inference, Fourier transforms, solving linear systems and real-time uncertainty quantification.

Bio: Dr. Sapan Agarwal is a Principal Member of Technical Staff at Sandia National Laboratories. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley, in 2012. He is leading projects to develop analog in-memory computing architectures to accelerate a variety of embedded applications at the point-of-sensing. His research interests include the co-design of computing systems from materials to algorithms, novel computing technologies, multiscale modeling of radiation effects, and explainable machine learning.

BETR Solid State Technology and Devices Seminar

Friday, September 2, 2022

Computing with Physical Systems

Peter McMahon

Assistant Professor
Applied and Engineering Physics
Cornell University

Abstract: With conventional digital computing technology reaching its limits, there has been a renaissance in analog computing across a wide range of physical substrates. In this talk I will introduce the concept of Physical Neural Networks [1] and describe a method my group has developed to train any complex physical system to perform as a neural network for machine-learning tasks. We have tested our method experimentally with three different systems – one mechanical, one electronic, and one photonic – and have been able to show MNIST handwritten-digit classification using each of these systems, despite the fact that none of the systems were initially designed to do machine learning. I will describe several possible future research directions on Physical Neural Networks, including the potential to create large-scale photonic accelerators for server-side machine learning [2], smart sensors that pre-process acoustic, microwave or optical signals in their native domain before digitization, new kinds of quantum neural network that don't require a carefully engineered quantum computer, and generally the prospect to endow analog physical systems with new, unexpected functionality.

[1] L.G. Wright, T. Onodera* et al. Nature 601, 549-555 (202 2)*
[2] T. Wang et al. Nature Communications 13, 123 (2022)

Bio: Dr. Peter McMahon is an assistant professor in Applied and Engineering Physics at Cornell University, where he has been since 2019. Prior to joining Cornell he completed his Ph.D. in Electrical Engineering and postdoctoral training in Applied Physics at Stanford University. He is the recipient of Packard and Sloan Fellowships, an Office of Naval Research Young Investigator Program Award and a Google Quantum Research Award, and is a CIFAR Azrieli Global Scholar in Quantum Information Science.

BETR Solid State Technology and Devices Seminar

Friday, September 16, 2022

Spin-Transfer-Torque MRAM: The Next Revolution in Memory

Daniel C. Worledge

Distinguished Research Staff Member
Senior Manager, MRAM
IBM Almaden Research Center

Abstract: Spin-Transfer-Torque MRAM was invented at IBM by John Slonczewski in the early 1990s. By using a spin-polarized current, instead of a magnetic field, to write a magnetic free layer in a magnetic tunnel junction, the required write current naturally decreases with area, providing attractive technology scaling. The discovery of high magnetoresistance in MgO tunnel barriers at IBM by Stuart Parkin, and later independently by Shinji Yuasa, enabled sufficient read signal to efficiently read magnetic tunnel junctions. The discovery of perpendicular magnetic anisotropy in thin CoFeB/MgO layers at IBM and independently by Tohoku University enabled a dramatic reduction in the switching current and opened the way to practical perpendicular magnetic tunnel junctions for dense Spin-Transfer-Torque MRAM. This talk will provide an overview of Spin-Transfer-Torque MRAM, including the three basic building blocks described above. I'll give an introduction to the basic physics of spin-transfer torque and applications of Spin-Transfer-Torque MRAM. Then I will review why perpendicular magnetic anisotropy is advantageous for MRAM compared to in-plane anisotropy, and the materials challenges of perpendicular anisotropy. I will discuss the research at IBM in 2009 that led to our discovery of perpendicular anisotropy in thin CoFeB/MgO layers, and our use of these layers to make the first practical perpendicular magnetic tunnel junctions and the first demonstration of reliable writing in Spin-Transfer-Torque MRAM. Finally, I will review our recent results on methods to lower the switching current of Spin-Transfer-Torque MRAM by using optimized magnetic materials and double magnetic tunnel junctions, including our recent demonstration of reliable 250 ps switching.

Bio: Dr. Worledge received a BA with a double major in Physics and Applied Mathematics from UC Berkeley in 1995, receiving the Department Scholar Award in physics and the Dorothea Klumpke Roberts Prize in mathematics. He then received a PhD in Applied Physics from Stanford University in 2000, with a thesis on spin-polarized tunneling in oxide ferromagnets, measuring the largest tunneling spin-polarization in (LaSr)MnO_3 and the first negative tunneling spin-polarization in $SrRuO_3$. After joining the Physical Sciences Department at the IBM T. J. Watson Research Center as a Post-doc in 2000, he became a Research Staff Member in 2001, inventing and developing Current-in-Plane Tunneling as a fast turn-around measurement method for magnetic tunnel junctions. In 2003, Dr. Worledge became the manager of the MRAM Materials and Devices group, and in 2013 he became Senior Manager of MRAM. In 2015 he was promoted to Distinguished Research Staff Member. He has worked on developing Toggle and then Spin Torque MRAM, including discovering perpendicular magnetic anisotropy in CoFeB|MgO, and leading the IBM team that developed perpendicular magnetic tunnel junctions and demonstrated the first integrated perpendicular spin torque MRAM, with ultra-low bit error rate. His current research interests include magnetic devices and their behavior at small dimensions, and new hardware approaches to machine learning. Dr. Worledge has received four IBM Outstanding Technical Achievement Awards, three IBM Outstanding Innovation Awards, and the IBM Research Client Award.

BETR Solid State Technology and Devices Seminar

Friday, September 23, 2022

Computing with p-Bits: Between a Bit and a q-Bit

Supriyo Datta

Thomas Duncan Distinguished Professor of Electrical and Computer Engineering
School of Electrical and Computer Engineering
Purdue University

Abstract: Digital computing is based on a deterministic bit with two values, 0 and 1. On the other hand, quantum computing is based on a q-bit which is a delicate superposition of 0 and 1. This talk draws attention to something in-between namely, a p-bit which is a robust classical entity fluctuating between 0 and 1. Feynman used the concept of a probabilistic computer as a counterpoint to the quantum computer, noting that " .. the only difference between a probabilistic classical world and the equations of the quantum world is that .. the probabilities would have to go negative .. " The power of quantum computing comes from exploiting these negative (more generally complex) probabilities, which in turn requires stringent experimental conditions to protect the phase. A probabilistic computer by contrast can be built with existing technology to operate at room temperature as we have demonstrated experimentally [1]. They lack the magic of complex probabilities but can function as hardware accelerators for many applications that use stochastic algorithms [2].

[1] https://www.nature.com/articles/s41586-019-1557-9
[2] https://ieeexplore.ieee.org/abstract/document/9393992

Bio: Dr. Supriyo Datta received his PhD from University of Illinois at Urbana-Champaign in 1979 working on surface acoustic wave devices, and has been with Purdue University since 1981. The non-equilibrium Green function (NEGF) method pioneered by his group provides the basis for the quantum simulation tools used in the semiconductor industry to design nano transistors. His innovative theoretical proposals have inspired new fields of research including spintronics, negative capacitance electronics and most recently the concept of probabilistic bits, or p-bits. He is also known for his books and online courses designed to disseminate the latest research results to a broad audience.

BETR Solid State Technology and Devices Seminar

Friday, September 30, 2022

Carbon Nanotube Transistors: Recent Progress Towards Applications in Highly-Scaled and High-Performance CMOS Logic

Greg Pitner

Technical Manager
Corporate Research Exploratory Devices
Taiwan Semiconductor Manufacturing Company (TSMC)

Abstract: Transistor innovations that combine emerging semiconductor channel materials and novel device component processing methods are the key enabler of continued speed and efficiency improvements in future CMOS technology nodes. Towards this goal, several decades of fundamental research on Carbon Nanotube (CNT) materials and devices have generated tremendous progress towards useful applications. In this talk we will first introduce the motivations and review the challenges towards utilizing semiconducting single-walled CNTs as a channel material in highly-scaled and high-performance CMOS transistors. We will then summarize recent experimental advances on CNT transistors by our team and collaborators including: (1) the lowest reported CNT contact resistance of 6.5 kΩ per CNT down to 10 nm contact length, (2) a novel method to deposit sub-3 nm high-capacitance gate dielectrics on CNT for excellent electrostatics down to 15 nm gate length, and (3) the first systematic study of band-to-band tunneling leakage in CNT MOSFETs which gives insight into the desired CNT bandgap for energy efficiency. We will conclude by describing from a transistor perspective the remaining challenges of CNT materials assembly and controlled CNT doping to encourage new research directions in the scientific community.

Bio: Dr. Greg Pitner received a B.S. in Electrical Engineering and Applied Physics from Rensselaer Polytechnic Institute in 2012, followed in 2018 by a M.S. and Ph.D. in Electrical Engineering from Stanford University. His Ph.D. research interest was improving CVD growth of densely aligned Carbon Nanotubes (CNT), and experimental device component prototyping towards low-resistance electrical contact to CNT channels to meet the needs of future transistor devices. During his academic career, Greg joined R&D teams at NASA, IBM, and IMEC for internships. Towards the end of his PhD, Greg co-founded a startup aiming to commercialize high-quality CNT wafers to enable R&D on a variety of customer applications. Three years ago Greg joined Taiwan Semiconductor Manufacturing Company (TSMC) in the Corporate Research Exploratory Devices team based in San Jose, CA. He is currently a Technical Manager leading a program focused on delivering fundamental advances in transistor device components built on 1D channel materials. His recent lead-author research has been published in IEDM, Nano Letters, Electron Device Letters, and Advanced Materials, with more than 30 collaborative co-authored papers published in scientific conferences and peer-reviewed journals including both Nature and Science.

BETR Solid State Technology and Devices Seminar

Friday, October 7, 2022

Intelligent Image-Activated Cell Sorting

Keisuke Goda

Professor
Department of Chemistry
University of Tokyo

Abstract: A fundamental challenge of biology is to understand the vast heterogeneity of cells, particularly how the spatial architecture of cells is linked to their physiological function. Unfortunately, conventional technologies such as fluorescence-activated cell sorting and the Coulter counter are limited in uncovering these relations and exploiting biomedical applications. In this talk, I will introduce Intelligent Image-Activated Cell Sorting, a new technology that performs real-time, intelligent, image-based sorting of cells at an unprecedented rate of >1000 cells per second (Nitta et al., Cell 2018; Isozaki et al., Nat. Protoc. 2019; Nitta et al., Nat. Commun. 2020; Mikami et al., Nat. Commun. 2020). This technology integrates high-throughput optical imaging, cell focusing, cell sorting, and deep learning on a hybrid software-hardware data-management infrastructure, enabling real-time automated operation for data acquisition, data processing, intelligent decision-making, and actuation. I will present a new class of applications in immunology, cancer biology, infectious disease, microbiology, and food science enabled by the technology.

Bio: Dr. Keisuke Goda is a professor in the Department of Chemistry at the University of Tokyo, an adjunct professor in the Institute of Technological Sciences at Wuhan University, and an adjunct professor in the Department of Bioengineering at UCLA. He obtained a B.A. degree from UC Berkeley summa cum laude in 2001 and a Ph.D. from MIT in 2007, both in physics. At MIT, he worked on the development of gravitational-wave detectors in the LIGO group which led to the 2017 Nobel Prize in Physics. After several years of work on high- speed imaging and microfluidics at Caltech and UCLA, he joined the University of Tokyo as a professor. His research group focuses on the development of serendipity-enabling technologies based on photonics, microfluidics, nanotechnology, and computational analytics to push the frontier of science (http://www.goda.chem.s.u-tokyo.ac.jp). He has published >300 journal and conference papers and received >30 awards including Japan Academy Medal, SPIE Biophotonics Technology Innovator Award, and Humboldt Foundation's Philipp Franz von Siebold Award to name a few.

BETR Solid State Technology and Devices Seminar

Friday, October 21, 2022

Fast-Tunable and Low-Loss Stress-Optical Microsystems

Sunil Bhave

Professor, Elmore Family School of Electrical and Computer Engineering
Faculty Director, Scifres Nanofabrication Facility
Purdue University

Friday, October 21, 2022
1:10-2:00 pm Pacific (Webex will start at 1:00 pm)

Abstract: Silicon Nitride (SiN) is an outstanding material for on-chip photonic systems because of its extremely low optical loss, outstanding optical power handling and controllable non-linearity. SiN photonic integrated circuits (PICs) are becoming more commonplace in high performance systems including LIDAR, Optical Frequency Combs, Spatial Light Modulators and Photonic Quantum Processors. In such microsystems, low-loss photonics enhances LIDAR resolution and range, octave-spanning combs for optical clocks, longer-distance free-space communication and higher intensity light incident on detectors in photonics quantum processors. However, modulation and tuning of SiN has been limited to thermal heaters because it's a dielectric amorphous material with no electro-optic coefficients. In this presentation I will present architectures based on piezoMEMS technology to demonstrate stress-optical modulation and tuning of silicon nitride optical ring resonators [1]. Specifically, I will demonstrate high speed tuning of self-injection locked lasers for LIDAR and frequency combs [2] and GHz frequency mechanical resonant actuators for implementing magnetic-free optical isolators [3,4]. If time permits, I will discuss optomechanical inertial sensors and microwave-to-optical quantum converters [5] in our Piezo-on-Nitride technology platform. This research is in close collaboration with Professor Tobias Kippenberg's group at EPFL.

1. H. Tian, J. Liu, B. Dong, J. C. Skehan, M. Zervas, T. J. Kippenberg, and S. A. Bhave, Nature Communications (2020).
2. J. Liu, H. Tian, E. Lucas, A. S. Raja, G. Lihachev, R. N. Wang, J. He, T. Liu, M. H. Anderson, W. Weng, S. A. Bhave, and T. J. Kippenberg, Nature (2020).
3. H. Tian, J. Liu, A. Siddharth, T. Blésin, T. J. Kippenberg, and S. A. Bhave, IEEE MEMS 2021, pp. 210-213.
4. H. Tian, J. Liu, A. Siddharth, R. N. Wang, T. Blésin, J. He, T. J. Kippenberg, and Sunil A. Bhave, Nature Photonics (2021).
5. T. Blésin, H. Tian, S. A. Bhave, and T. J. Kippenberg, Physical Review A (2021).

Bio: Professor Sunil Bhave received the B.S. and Ph.D. degrees from Cal in EECS in 1998 and 2004 respectively. In April 2015, he joined the Elmore Family School of Electrical and Computer Engineering at Purdue University where he is currently the Faculty Director of the Scifres Nanofabrication Laboratory. Sunil received the NSF CAREER Award in 2007, the DARPA Young Faculty Award in 2008, the IEEE Ultrasonics Society's Young Investigator Award in 2014 and the Google Faculty Research Award in 2020. His students have received Best Paper Awards at MEMS 2021, IFCS 2021, IFCS 2020, IEEE Photonics 2012, Ultrasonics 2009, and IEDM 2007. Before joining Purdue, Sunil was an associate professor at Cornell and sensor architect at Analog Devices.

BETR Solid State Technology and Devices Seminar

Friday, October 28, 2022

Carbon Nanotube Transistors for a Future 3D Logic Technology

H.-S. Philip Wong
Willard R. and Inez Kerr Bell Professor
Department of Electrical Engineering
Stanford University

Abstract: Carbon Nanotube (CNT) Field-Effect Transistors (CNFETs) are promising candidates for future high-performance and energy-efficient digital logic. Gate-All-Around (GAA) CNFETs with doped extensions and multiple layers of high-density CNTs are projected to show up to 7× Energy-Delay Product (EDP) benefits vs. Si FET at the 2 nm technology node [1]. Moreover, CNFETs have already been integrated into silicon industrial manufacturing facilities at relaxed nodes (e.g. through DARPA 3DSoC program, at ADI, and SkyWater Technology Foundry), thus illustrating compatibility with existing fab process infrastructures [2-3]. Many fundamental building blocks of the CNFET technology have already been demonstrated. In the very near future, it will be possible to integrate all the building blocks achieved thus far to demonstrate a MOSFET-like structure with 35-nm contacted gate pitch, and 20-nm active width that is projected to have performance that far exceeds Si transistors for a 2-nm node logic technology while at the same time can be fabricated in multiple 3D device layers for a future logic technology. In this talk, I will describe the journey of the worldwide CNT research community that leads up to this important juncture. I will discuss the remaining challenges for CNFET to mature into a manufacturing- ready technology.

[1] C. Gilardi et al., "Extended Scale Length Theory Targeting Low-Dimensional FETs for Carbon Nanotube FET Digital Logic Design-Technology Co-optimization," 2021 IEEE International Electron Devices Meeting (IEDM), 2021, pp. 27.3.1-27.3.4, doi: 10.1109/IEDM19574.2021.9720672.
[2] T. Srimani et al., "Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry: Multi-Tier Complementary Carbon Nanotube Logic and Resistive RAM at a 130 nm node," 2020 IEEE Symposium on VLSI Technology, 2020, pp. 1-2, doi: 10.1109/VLSITechnology18217.2020.9265083.
[3] M. D. Bishop et al., "Fabrication of carbon nanotube field-effect transistors in commercial silicon manufacturing facilities," Nature Electronics 3, 2020, pp. 492–501, doi: 10.1038/s41928-020-0419-7.

Bio: Dr. H.-S. Philip Wong is the Willard R. and Inez Kerr Bell Professor in the School of Engineering at Stanford University. He joined Stanford University as Professor of Electrical Engineering in 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. From 2018 to 2020, he was on leave from Stanford and was the Vice President of Corporate Research at TSMC, the largest semiconductor foundry in the world, and since 2020 remains the Chief Scientist of TSMC in a consulting, advisory role. He is a Fellow of the IEEE and received the IEEE Electron Devices Society J.J. Ebers Award, the society's highest honor to recognize outstanding technical contributions to the field of electron devices that have made a lasting impact, as well as the IEEE Andrew S. Grove Award, the IEEE Technical Field Award to honor individuals for outstanding contributions to solid-state devices and technology. He is the founding Faculty Co-Director of the Stanford SystemX Alliance – an industrial affiliate program focused on building systems, the faculty director of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI), and the faculty director of the Stanford Nanofabrication Facility.

BETR Solid State Technology and Devices Seminar

Friday, December 2, 2022

Designing Artificial Synapses for Application-Specific Neuromorphic Computing Using Magnetic and 2D Materials

Jean Anne Incorvia

Assistant Professor and Fellow of Advanced Micro Devices (AMD) Chair in Computer Engineering
Department of Electrical and Computer Engineering
The University of Texas at Austin

Abstract: As we look to the future of computing in immersive environments for edge applications, new materials, devices, and circuits provide new ways to efficiently compute. In particular, hardware-aware neuromorphic computing takes inspiration from the brain to encode information in bio-mimetic artificial synapses and neurons assembled into neural networks. Most simply, an artificial synapse should have controllable resistance levels to set the connectivity between neurons. Features of linearity in the weight change and symmetric response to positive and negative weight updates are also desirable for efficient neural network training. But, if we can add additional features to the synapses themselves, inspired by the features of the brain, these can lead to system-level benefits depending on the application. I will present my group's work on designing, building, and measuring artificial synapses using both magnetic materials and atomically thin (2D) materials. By electrically controlling a magnetic domain wall (DW) underneath a magnetic tunnel junction (MTJ) memory element, we show 3-5 controllable weight states that are highly stable at room temperature [1]. Tuning the device geometry in turn tunes the metaplastic behavior of the synapse, allowing application-specific design for either inference or online learning. We will show how this DW-MTJ artificial synapse can satisfy the necessary requirements for artificial neural networks integrated with CMOS. I will then show our results on designing bilayer graphene transistors as artificial synapses that are constructed from fully bio-compatible materials, respond in biologically-relevant timescales, and have ultra-low switching energy [2]. The graphene artificial synapses also show unique metaplasticity that can be used to outperform ideal linear synapses in classification tasks. Such devices are strong candidates for bio-interfaced neuromorphic computing. These results show the impact new materials can have as we encounter new computing needs.

[1] T. Leonard, S. Liu, M. Alamdar, H. Jin, C. Cui, O. G. Akinola, L. Xue, T. P. Xiao, J. S. Friedman, M. J. Marinella, C. H. Bennett, and J. A. C. Incorvia. *Advanced Electronic Materials,* 2200563 (2022).
[2] D. Kireev, S. Liu, H. Jin, T. P. Xiao, C. H. Bennett, D. Akinwande, and J. A. C. Incorvia. *Nat. Commun.* 13, 4386 (2022).

Bio: Dr. Jean Anne C. Incorvia is an Assistant Professor and holds the Fellow of Advanced Micro Devices (AMD) Chair in Computer Engineering in the Department of Electrical and Computer Engineering at The University of Texas at Austin, where she directs the Integrated Nano Computing (INC) Lab. Dr. Incorvia develops practical nanodevices for the future of computing using emerging physics and materials. Dr. Incorvia received her bachelor's in physics from UC Berkeley in 2008 and her Ph.D. in physics from Harvard University in 2015, cross-registered at MIT. From 2015-2017, she completed a postdoc at Stanford University. She has over 60 articles published in peer-reviewed journals and conference proceedings and has given over 60 invited talks. She received a 2020 US National Science Foundation CAREER award, the 2020 IEEE Magnetics Society Early Career Award, and a 2021 Intel Rising Stars award. She was an invited contributor to the 2020 and 2022 IEEE International Roadmap for Devices and Systems (IDRS). She is serving on the administrative committee of the IEEE Magnetics Society, and she has served on and taken leadership roles in the International Electron Devices Meeting (IEDM), the Device Research Conference (DRC), the Magnetism and Magnetic Materials Conference (MMM), and Intermag.

BETR Solid State Technology and Devices Seminar

Friday, January 27, 2023

Strain Engineering 2D van der Waals Devices

Stephen M. Wu

Assistant Professor
Department of Electrical and Computer Engineering
Department of Physics and Astronomy
University of Rochester

Abstract: Strain engineering in electronics has been widely utilized over the last 20 years to enhance carrier mobility in most standard Si-based CMOS fabrication processes. These process-induced strain engineering techniques, engineered from the nanofabrication process itself, are simple, reliable, applied device-to-device, and highly scalable down to the nanometer scale. In this talk, I will introduce our groups work in exploring how process-induced strain engineering translates to the world of 2D materials, and how this may be applied to engineer novel electronic devices and control quantum materials properties. Control over the strain degree-of-freedom in 2D materials opens new pathways for exploration in engineered quantum materials and devices, since the level of control over strain in weakly-bonded 2D systems can go far beyond strain-engineering in conventional 3D-bonded materials. This will be discussed in the context of three different ongoing projects in our group: 2D straintronic phase-change transistors/memristors, moiré superlattice engineering with strain in twisted bilayer 2D heterostructures, and strain-controllable edge state superconductivity in 2D topological Weyl semimetals.

Bio: Dr. Stephen M. Wu is an Assistant Professor at the University of Rochester in the Department of Electrical and Computer Engineering and the Department of Physics and Astronomy. His research interests involve engineering quantum materials to create novel electronic or quantum devices. For work in this area, he has won the NSF CAREER award in 2020. Before Rochester, he was a postdoctoral researcher at Argonne National Laboratory within the Materials Science Division. He received his Ph.D. in Physics, B.S. in Electrical Engineering and Computer Science, and B.A. in Physics all from the University of California, Berkeley.

BETR Solid State Technology and Devices Seminar

Friday, February 3, 2023

Nanophotonics-Enabled Infrared Microspectrometers and Optical Tweezers

Kenneth Crozier

Professor of Physics and Electronic Engineering
Deputy Director, ARC Centre of Excellence for Transformative Meta-Optical Systems
The University of Melbourne

Abstract: We discuss two applications of engineering light-matter interactions at the nanoscale. The first is for optical tweezers. One half of the Nobel Prize in Physics for 2018 was awarded to A. Ashkin for optical tweezers, which use the forces exerted by light to trap and manipulate particles. Conventional optical tweezers employ lenses to focus laser beams, but these can only focus light to spots no smaller than roughly half the wavelength. This makes it challenging to trap very small particles. We overcome this limitation by using nanostructures, rather than lenses, to concentrate light. We discuss our recent work on the use of algorithms to design nanostructures for optical tweezers. The second application is for chip-scale infrared microspectrometers. The identification of chemicals from their mid-infrared spectra has numerous applications. This is generally done using laboratory benchtop tools. Although such systems offer high performance, alternative platforms offering reduced size, weight, and cost can enable a host of new applications. Here a compact microspectrometer platform for chemical identification, comprising a mid-infrared metasurface integrated with a lightweight (≈1 g) and very small (≈1 cm^3) microbolometer-based thermal camera is experimentally demonstrated.

Bio: Dr. Kenneth Crozier is Professor of Physics and Electronic Engineering at the University of Melbourne. He is also Deputy Director of the Australian Research Council (ARC) Centre of Excellence for Transformative Meta-Optical Systems. Prior to joining the University of Melbourne, he was an associate professor at Harvard University. He received his undergraduate degrees in Electrical Engineering and Physics at the University of Melbourne. He received his MSEE and PhD in Electrical Engineering from Stanford University. In 2008, he received a CAREER Award from the National Science Foundation (USA) and a Loeb Chair at Harvard, an endowed position for junior faculty. He returned to Australia in 2014. In that year, he was awarded an Innovation Fellowship from VESKI (Victorian Endowment of Science, Knowledge, and Innovation) and a Future Fellowship from the ARC.

BETR Solid State Technology and Devices Seminar

Friday, February 17, 2023

Hardware Challenges in Fault-Tolerant Photonic Quantum Computing

Youngik Sohn

Assistant Professor
School of Electrical Engineering
Korea Advanced Institute of Science and Technology (KAIST)

Abstract: Photonic quantum computing is going to work on measurement-based quantum computing scheme, which is inspired by the quantum teleportation. Implementation of such measurement-based operation is called 'feed-forward' from hardware perspective, and it is the core building block to realize fault-tolerant photonic quantum computing. In this seminar, I will discuss the key aspects of such feed-forward system components and remaining challenges in its development.

Bio: Dr. Youngik Sohn is an assistant professor in the School of Electrical Engineering at Korea Advanced Institute of Science and Technology (KAIST). He studied Electrical Engineering for his Bachelor's and Master's degrees from Seoul National University and Stanford University, respectively. In 2018, he received Ph.D. degree in Applied Physics from Harvard University by his pioneering contribution to developing MEMS technology for quantum emitters in diamond. After receiving the degree, he has joined an early phase startup called PsiQuantum, which now became one of the leading quantum computer manufacturers in the world. After joining KAIST in 2020, he continues to work on chip-scale quantum technologies.

BETR Solid State Technology and Devices Seminar

Friday, February 24, 2023

Mechanistic Understanding Coupled with the Discovery of Multifunctional Energy Materials

Carolin M. Sutter-Fella

Staff Scientist
Molecular Foundry
Lawrence Berkeley National Laboratory

Abstract: From the Stone Age to today's Silicon Age, materials have had a historical impact on society and their manipulation has been the engine of societal advancement. With the ultimate goal to transition society to sustainable energy technologies and to improve our collective quality of life, there is a need for novel functional materials. This includes the discovery of new materials, understanding, controlling and manipulating their assembly and resulting functional properties on different time and lengths scales. In this talk I will introduce state-of-the-art in situ multimodal synthesis capabilities to characterize the chemical transformation of solution processed halide perovskite thin films for photovoltaic, LED, and detector applications amongst others. Establishing the relationships between synthesis condition and film properties will enable active control of synthesis parameters and increase reproducibility. The formation of halide perovskites from colloidal precursors including the initial stages of formation and the physicochemical evolution of properties via polydisperse nanocrystal nucleation and solvent-complexation will be discussed. We identified for example how the precursor and antisolvent influence the crystallization pathway, how morphology can be templated, and how additives can aid room temperature processing. By correlating diffraction and photoluminescence (PL) measurements, it will be demonstrated how in situ PL can reveal subtle changes throughout all synthesis steps. Lastly, I will describe our joint effort in setting up a robotic platform, SpinBot One, to synthesize and characterize halide perovskite films coupled to neural networks which learn time-dependent processes to optimize the optical properties of the material under study. SpinBot One fabricates halide perovskite thin films via spin coating and thermal annealing followed by build-in optical characterization (UV Vis, photoluminescence) and external X-ray diffraction measurements. Ultimately, coupling automated synthesis platforms with in situ characterization will enable autonomous experimentation and materials discovery with unprecedented pace.

Bio: Dr. Carolin M. Sutter-Fella is a Staff Scientist in the Molecular Foundry at the Lawrence Berkeley National Laboratory (LBNL). Before joining the Foundry she built her research program enabled by LBNL's Glenn Seaborg Early Career Fellowship (2017). Her research focuses on synthesis of functional materials and understanding synthesis-property relationships using multimodal in situ techniques as well as development of an automated thin film synthesis and characterization platform. She received her Ph.D. in Electrical Engineering from ETH Zürich, Switzerland, in 2014 where she worked on the synthesis of chalcogenide thin film solar cells. Before joining LBNL, she was a Swiss NSF postdoctoral fellow at UC Berkeley.

BETR Solid State Technology and Devices Seminar

Friday, March 10, 2023

Sustainability and the Future of Semiconductor Innovations

Dr. Carolyn R. Duran

Vice President and Engineering Manager
Components Research
Intel Corporation

Abstract: The semiconductor industry has a great track record of driving innovations in the pursuit of Moore's Law, focused on performance and cost. However, in recent times we have recognized that delivering to Moore's Law is **necessary** but **not sufficient** for our collective futures, and we need to simultaneously solve for sustainability. In her talk, Dr. Duran will share Intel's approach to environmental stewardship and committed goals. Within that framework, Dr. Duran will focus on critical materials and process research areas that can affect positive change. Collectively, our industry, in partnership with academia, can deliver the promise of world-changing technologies while changing the world for the better.

Bio: Dr. Carolyn R. Duran is a Vice President and Engineering Manager in Components Research at Intel Corporation. In this role, Carolyn leads advanced process and materials research to invent, develop and demonstrate viable revolutionary technologies necessary for Intel's continued leadership in the industry. Over her 24-year career, Duran's scope has spanned technology development, supply chain, including responsible minerals, and a corporate charter enabling memory and IO technologies in the product groups. Duran is currently serving as the Immediate Past President of the Materials Research Society and is an adjunct professor of Materials Science and Engineering at Northwestern University. A recognized industry leader, Duran was named on *Fast Company's* "Most Creative People in Business 1000" list in 2016 and ranked no. 2 on *Business Insider's* "Most Powerful Women Engineers in the World" list in 2014. Duran received her bachelor's degree in materials science and engineering from Carnegie Mellon University and her Ph.D. in the same field from Northwestern University. She holds five patents in the area of semiconductor process engineering.

BETR Solid State Technology and Devices Seminar

Friday, March 17, 2023

Defects, Devices, and Degradation of Metal Halide Perovskites: An Electrochemist's Perspective

Erin L. Ratcliff

Associate Professor
Chemical and Environmental Engineering
University of Arizona

Abstract: Defects are considered one of the most prominent contributions to diminished power conversion efficiencies and long-term stability in printable metal halide perovskite materials and optoelectronic devices. Defects can arise from a combination of point defects, grain boundaries, charge transfer with Lewis acid/base sites at the contacts, and/or mobile redox-active halides. Thus, every perovskite composition and contact choice can result in differences in defect distributions.

Defect states have most often been characterized using electrical, optical, and magnetic techniques; however, independently assessing donor and acceptor defect quantities and energetics using a direct experimental approach with few empirical assumptions can be challenging. Realization of high-performing and long-term stable devices requires a combination of method advancement for the quantification of defects and mitigation strategies. This talk will discuss emerging electrochemistry-based measurement science approaches to quantify the distribution and energetics of donor and acceptor defects in a prototypical perovskite solar cell material $(FA_{.79}MA_{.16}Cs_{.05})Pb(I_{.87}Br_{.13})_3$ (or $Cs_{.05}FA_{.79}MA_{.16}$), with demonstrations of the methodology to other perovskite active materials. We utilize a solid-state electrolyte top contact to create "half-cells" of device-relevant material stacks under realistic electric fields. This allows us to spectroscopically assess onsets in valence and conduction bands under conditions of operando, as well as quantify near-band defects using redox probes. Connections to device performance, including modifications to the near-surface region of hole-transporting layers (i.e. NiOx), will be provided as well as preliminary results to understand degradation pathways using near-ambient pressure x-ray photoelectron spectroscopy and operando x-ray scattering. Collectively, this developed tool-suite provides a holistic approach to understand defects, device performance and stability in this exciting class of materials.

Bio: Dr. Erin Ratcliff is an Associate Professor of Chemical and Environmental Engineering at the University of Arizona, with courtesy appointments in Materials Science and Engineering and Chemistry and Biochemistry and holds a joint appointment at the National Renewable Energy Laboratory. She earned a B.A. in Chemistry, Mathematics, and Statistics in 2003 from St. Olaf College in Northfield, MN and a PhD in Physical Chemistry from Iowa State University in 2007. Her group "Laboratory for Interface Science for Printable Electronic Materials" uses a combination of electrochemistry, spectroscopies, microscopies, and synchrotron-based techniques to understand fundamental structure-property relationships of next-generation materials. Materials of interest include metal halide perovskites, π-conjugated materials, colloidal quantum dots, and metal oxides. Current research is focused on mechanisms of electron transfer and transport across interfaces, including semiconductor/electrolyte interfaces and durability of printable electronic materials. Prof. Ratliff is also the Director of the newly funded Energy Frontier Research Center (EFRC) entitled "Center for Soft PhotoElectroChemical Systems (SPECS)" and the co-director for the Institute for Energy Solutions at the UArizona. She has received several awards for her research and teaching, including the 2023 Da Vinci Fellow, 2022 College of Engineering Researcher of the Year award, The Ten at Ten People of Energy Frontier Research Centers DOE Basic Energy Sciences award in 2019, Most Supportive Junior Faculty Member in Materials Science (2019), and Senior Summer Faculty Research Fellow at the Naval Research Laboratory (2020, 2021).

BETR Solid State Technology and Devices Seminar

Friday, March 24, 2023

Large Scale Optical Switching in Google Data Centers

Dr. Kevin Yasumura

Principal Engineer/Director
Platforms Optics Team
Google LLC

Abstract: In this talk we present, to the best of our knowledge, the first large-scale production deployment of optical circuit switches for datacenter networking. Over the last decade, we have evolved our datacenter network fabric to a direct-connect topology between the machine aggregation blocks. Critical architectural changes for this include: a datacenter interconnection layer employing micro-electro-mechanical systems (MEMS) based optical circuit switches (OCSes) to enable dynamic topology reconfiguration, centralized software-defined networking (SDN) control for traffic engineering, and automated network operations for incremental capacity delivery and topology engineering.

Bio: Dr. Kevin Yasumura is a Principal Engineer/Director in Google's Platforms Optics Team. At Google he is the Technical Lead for MEMS and optical switching development. He has over 25 years of experience developing MEMS-based products and systems. Before joining Google, he was a founding member and Manager of Micro-machining Development at Iolon Corporation where they developed MEMS tunable lasers, tunable filters, and optical switches. He was also Senior Director of Product Development at Formfactor where he led the development of MEMS-based integrated circuit test solutions. Kevin holds a bachelor's degree in physics from U.C. Berkeley where he worked on laser atom trapping in Prof. Stuart Freedman's research group. He also holds an M.S. and Ph.D. in applied physics from Stanford University.

BETR Solid State Technology and Devices Seminar

Friday, April 7, 2023

The Berkeley Surface Emitting Laser (BerkSEL): A Scale-Invariant Laser?

Boubacar Kanté

Chenming Hu Endowed Chaired Associate Professor
Electrical Engineering and Computer Science
University of California, Berkeley

Abstract: The scaling of lasers and in-particular of surface emitting lasers is a multi-decade long question that has been investigated since the invention of lasers in 1958. It is an important question with numerous applications. In this talk, I will propose and discuss an intriguing solution to this question. The first part of the talk will briefly discuss my group's invention of topological lasers [1-3]: integrable non-reciprocal coherent light sources as well as compact bound state in continuum sources [4]. The second part of the talk will discuss a single aperture that is in principle infinitely scalable and that solves the optics challenge of single apertures scaling. I will discuss the physics of the invention that I named Berkeley Surface Emitting Laser (BerkSEL) [5].

[1] B. Bahari, A. Ndao, F. Vallini, A. El Amili, Y. Fainman, and B. Kanté, Science 358, 636 (2017).
[2] B. Bahari, L. Hsu, S. H. Pan, D. Preece, A. Ndao, A. El Amili, Y. Fainman, and B. Kanté, "Photonic quantum Hall effect and multiplexed light sources of large orbital angular momenta", Nature Physics 17, 700–703 (2021).
[3] W. Noh, H. Nasari, H.-M. Kim, Q. Le-Van, Z. Jia, C.-H. Huang, and B. Kanté, "Experimental demonstration of single-mode topological valley-Hall lasing at telecommunication wavelength controlled by the degree of asymmetry," Optics Letters 45 (15) 4108–4111 (2020).
[4] A. Kodigala, T. Lepetit, Q. Gu, B. Bahari, Y. Fainman, and B. Kanté, "Lasing Action from Photonic Bound States in Continuum," Nature 541, 196 – 199 (2017).
[5] Rushin Contractor, Wanwoo Noh, Walid Redjem, Wayesh Qarony, Emma Martin, Scott Dhuey, Adam Schwartzberg & Boubacar Kanté, Nature 608, 692–698 (2022).

Bio: Dr. Boubacar Kanté is an associate professor of Electrical Engineering and Computer Sciences (EECS) at the University of California Berkeley and a faculty scientist at the materials science division (MSD) of the Lawrence Berkeley National Laboratory (LBNL). In 2010, he received a Ph.D degree in Engineering/Physics from "Université de Paris Sud" (Orsay-France). He was assistant professor and then associate professor of Electrical and Computer Engineering (ECE) at UC San Diego from 2013 to 2018. His research interests include wave-matter interaction and nano-optics. Boubacar Kanté is a 2021 Bakar Fellow and a 2020 Moore Inventor Fellow. He received the 2017 Office of Naval Research (ONR) Young Investigator Award, the 2016 National Science Foundation (NSF) Career Award, The best undergraduate teacher award from UC San Diego Jacob School of Engineering in 2017, the 2015 Hellman Fellowship, the Richelieu Prize in Sciences from the Chancellery of Paris Universities for the best Ph.D in France in Engineering, Material Science, Physics, Chemistry, Technology in 2010, the Young Scientist Award from the International Union of Radio Science (URSI) in Chicago in 2007, the Fellowship for excellence from the French Ministry of Foreign Affairs in 2003 for his undergraduate studies, a Research Fellowship from the French Research Ministry for his Ph.D. studies.

BETR Solid State Technology and Devices Seminar

Friday, April 14, 2023

Carbazole Based Self-assembly Monolayers for Highly Efficient Sn/Pb-Perovskite Solar Cells

Maria Antonietta Loi
Professor of Photophysics and Optoelectronics
Zernike Institute for Advanced Materials
University of Groningen, Netherlands

Abstract: Mixed Tin/Lead (Sn/Pb) perovskites have the potential to achieve higher performances in single junction solar cells than Pb-based compounds. The best Sn/Pb based devices are fabricated in the p-i-n structure and frequently PEDOT: PSS is utilized as hole transport layer, even if there are many doubts on a possible detrimental role of this conductive polymer. Here, we propose the use of [2-(9H-Carbazol-9-yl)ethyl]phosphonic acid (2PACz) and the functionalized [2-(3, 6-dibromo-9H-carbazol-9-yl) ethyl] phosphonic acid (Br-2PACz) version, as substitutes for PEDOT: PSS. By using Br-2PACz as HTL we achieve record efficiency (19.51%) with the perovskite composition $Cs_{0.25}FA_{0.75}Sn_{0.5}Pb_{0.5}I_3$ without any anti-reflective coating. The halogen functionalization of the SAMs is an efficient way to improve both the device performances and stability. Several factors seem to determine these improvements. The two carbazole-based molecules are able to form a self-assembled monolayer which show minimal parasitic absorption and low charge recombination when compared to PEDOT: PSS films. Additionally, the perovskite layer deposited on SAMs show a higher crystallinity, with reduced pinhole density and larger grains. The defect density for the perovskite films was also reduced when deposited on Br-2PACz or 2PACz compared to PEDOT: PSS. PL and TRPL measurements further confirmed the better perovskite film quality when deposited on SAMs, with reduced charge recombination. Finally, the wettability of the perovskite precursor solution on top of the SAMs is a problem which limits SAMs application in Sn- or mixed Sn/Pb-perovskite solar cells on a large scale, limiting enormously the yield of device fabrication. I will present a solution for this issue, that may allow to improve both the scalability and reproducibility of the SAMs-based perovskite solar cell.

Bio: Dr. Maria Antonietta Loi studied physics at the University of Cagliari in Italy where she received the PhD in 2001. In the same year she joined the Linz Institute for Organic Solar cells, of the University of Linz, Austria as a postdoctoral fellow. Later she worked as researcher at the Institute for Nanostructured Materials of the Italian National Research Council in Bologna Italy. In 2006 she became assistant professor and Rosalind Franklin Fellow at the Zernike Institute for Advanced Materials of the University of Groningen, The Netherlands. She is now full professor in the same institution and chair of the Photophysics and OptoElectronics group and head of the Department of Mathematics and Natural Sciences of the University College of the University of Groningen. She has published more than 240 peer review articles in photophysics and optoelectronics of nanomaterials. She is cluster leader “Functional materials” of M2i. She serves Deputy editor of Applied Physics Letters, and she is member of the international advisory board of several international journals. In 2013 she has received an ERC starting Grant. In 2020 she became fellow of the American Physical Society.

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Spring 2022 Workshop – On-Campus Event

Tuesday, May 31, 2022

Hearst Mining Memorial Building, Room 290

All times are Pacific Daylight Time

10:45 AM	*Registration & Badge Pickup*	
11:00 AM	Closed Session for Corporate Affiliates *(Working Lunch)*	
	- Opening Remarks	Tsu-Jae King Liu
	- Corporate Affiliates Dialog with the BETR Center	Jeffrey Bokor (Moderator)
12:00 PM	Open Session: Welcome	
12:05 PM	BETR Presentations (Block 1)	
	- "Room-temperature Deposited Tellurium Thin Films for p-type Field-effect Transistors, Circuits, and Photodetectors"	Ali Javey
	- "Ultra-low EOT Gate Oxide Using Ferroelectric HfO_2-ZrO_2 Superlattice"	Sayeef Salahuddin
	- "Voltage and Current Controlled Nanomagnetism for Memory and Logic"	Ramamoorthy Ramesh
	- "Progress Towards Picosecond On-chip Magnetic Memory"	Jeffrey Bokor
1:45 PM	*Break*	
2:05 PM	BETR Presentations (Block 2)	
	- "Electronic-Photonic Systems-on-Chip"	Vladimir Stojanović
	- "Large-scale Silicon Photonic MEMS Switches"	Johannes Henriksson
	- "Computational Microscopy"	Laura Waller
3:20 PM	*Break*	
3:45 PM	Student & Postdoc Poster Session	
5:00 PM	*Adjournment*	

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Spring 2022 Workshop – Online Event

Thursday, May 26, 2022 (All times are Pacific Daylight Time)

Zoom: ***https://berkeley.zoom.us/j/91943002304?pwd=WDVtRTF5aGtGdUV1S0N5T3d1VHRqUT09***

Password: BETRmeet

4:00 PM	Welcome Remarks	Michael Bartl
4:05 PM	BETR Presentations (Part 1)	
	"Effect of Ultrafast Laser Heating on Electrical Switching of LCO Devices"	Hanuman Singh (Bokor group)
	"The Spin Hall Effect in Epitaxial Oxide Heterostructures of BPBO and LSMO"	Isaac Harris (Ramesh group)
	"Non-volatile Ferroelectrically Controlled Spin Transport in Multiferroic $BiFeO_3$ at Room Temperature"	Xiaoxi Huang (Ramesh group)
	"Physical Limits of Ferroelectricity and Negative Capacitance for Equivalent Oxide Thickness Scaling"	Suraj Cheema (Salahuddin group)
	"Reliability and Ultrafast Characterization of Negative Capacitance HfO_2-ZrO_2 Gate Stack"	Nirmaan Shanker (Salahuddin group)
	"Demonstration of Low EOT Gate Stack and Record Transconductance on L_g=90 nm nFETs Using 1.8 nm Ferroic HfO_2-ZrO_2 Superlattice"	Li-Chen Wang (Salahuddin group)
	"Tin Perovskites with 2D/3D Structure"	Maykel Nijenhuis (Arias group)
4:40 PM	Breakout into Small-Group Discussions (Zoom Rooms); Part 1	
5:25 PM	*Break*	
5:35 PM	BETR Presentations (Part 2)	
	"Multianalyte Biodegradable Sensor Arrays for Precision Agriculture"	Nithila Poongovan (Arias group)
	"Semiconductor Negative Differential Resistance (NDR) Device for Compact Integrated Circuits"	Lars Tatum (Liu group)
	"Optically Switchable Nanoscale Magnetic Tunnel Junction"	Sucheta Mondal (Bokor group)
	"Integrated Optical MEMS for Scalable Trapped Ion Quantum Computing"	Daniel Klawson (Wu group)
	"Dynamic Spectrum Optoelectronics with Black Phosphorus"	Naoki Higashitarumizu (Javey group)
	"Electronic-Photonic System for Massive-MIMO mm-wave Applications"	Ruocheng Wang (Stojanović group)
	"High-Voltage IC Design for High-Radix Silicon Photonic MEMS Switches"	Erik Anderson (Stojanović group)
	"Nanoscale Contact Welding for Programmable Relays"	Tsegereda Esatu (Liu group)
6:15 PM	Breakout into Small-Group Discussions (Zoom Rooms); Part 2	
7:00 PM	*Adjournment*	

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Fall 2022 Workshop & Technical Advisory Board Meeting

Thursday, November 3, 2022

Hearst Memorial Mining Building, Room 290

9:45 AM	*Registration & Badge Pickup*	
10:00 AM	Closed Session for Corporate Affiliates (Technical Advisory Board)	
	- Opening Remarks and BETR Overview by Tsu-Jae King Liu and Michael Bartl	
	- Corporate Affiliates Dialog with the BETR Center, facilitated by Jeffrey Bokor	
11:00 AM	*Lunch*	
12:00 PM	Open Session: Welcome	
12:05 PM	BETR Presentations (Block 1)	
	- "Silicon Photonics for Optical Switching, 3D Sensing, and Quantum Computing"	Ming Wu
	- "Simulation-Based Comparison of iFinFET and Nanosheet FET 3nm-Node Transistor Designs"	Tsu-Jae King Liu
	- "Hardware-Accelerated Boltzmann for Intractable Problems"	Saavan Patel
1:05 PM	*Break*	
1:25 PM	Panel Discussion	
	"The Role of Internships in Workforce Development: Opportunities and Challenges"	Laura Waller (Moderator)
	Panelists: Nerissa Draeger (Lam Research), Uygar Avci (Intel), Philip Kraus (Applied Materials), Han Wang (TSMC), Yach Lai (Cadence)	
2:25 PM	*Break*	
2:45 PM	BETR Presentations (Block 2)	
	- "Onsager Computing – Optimization by the Principle of Minimum Heat Generation"	Eli Yablonovitch
	- "Generating Domain-Specific Systems at Scale"	Sophia Shao
	- "Printed Flexible Electronic Systems"	Ana Arias
3:45 PM	*Break*	
4:00 PM	Student & Postdoc Poster Session	
5:30 PM	*Adjournment*	