Sarika Madhvapathy

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Education - University of California, Berkeley

PhD Student, Electrical Engineering and Computer Sciences *(GPA: 3.95)* *August 2021 – Present*

MS, Electrical Engineering and Computer Sciences *(GPA: 3.93)* *May 2021*

BS, Electrical Engineering and Computer Sciences *(GPA: 3.69)* *May 2020*

Selected Coursework: Microelectronic Devices, Semiconductor Physics, Integrated Circuits, Advanced Integrated Circuits, Data Converters, Digital IC Design, Advanced Digital IC Design, Signals and Systems, Digital Signal Processing, Probability, Random Processes, Operating Systems, Machine Learning, Linear Systems, Information Theory, Deep Reinforcement Learning, Data Structures, Computer Architecture, Robotics, Computer Security

Technical Skills: Analog Design, Programming/Scripting, PCB Design, Machine Learning, Digital Design

Licenses: Amateur Radio Technician License (callsign KN6IEP), *March 2020 – Present*

Software: Cadence Virtuoso, Altium Designer, Xilinx ISE, Xilinx Vivado, MATLAB, JMP

Proficient Languages: Python, Verilog, C, Java

Research

Graduate Research Assistant, Berkeley Wireless Research Center *August 2020 – Present*

- Investigating the use of silicon photonics for biomedical applications, in particular sensors for endoscopic ultrasound using silicon mircoring resonators (MRRs) in the Integrated Systems Group advised by Prof. Vladimir Stojanovic
- Design and tape out (in a 45nm SOI process) photonic layouts using Berkeley Photonic Generator (BPG), a Python-based layout automation tool
- Write FPGA processing code to test MRR sensor arrays and post-process data using Verilog and Vivado Design Suite
- Designed PCBs to measure and test high speed chip outputs, conducted experiments to characterize ultrasound transducer sensitivity

Undergraduate Research Assistant, Berkeley Wireless Research Center *September 2018 – May 2020*

- Assisted in porting circuit blocks for an optical receiver to the 14-nanometer FINFET design process using Berkeley Analog Generator (BAG), a Python-based CMOS layout automation tool, in the Integrated Systems Group

Publications

- P. Zarkos, S. Buchbinder, C. Adamopoulos, **S. Madhvapathy**, O. Hsu, J. Whinnery, P. Bhargava, and V. Stojanović, "Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Applications in a Zero-Change 45-nm CMOS-SOI Process," in *IEEE Journal of Solid-State Circuits*, doi: 10.1109/JSSC.2022.3222829.
- P. Zarkos, S. Buchbinder, C. Adamopoulos, **S. Madhvapathy**, O. Hsu, J. Whinnery, P. Bhargava, and V. Stojanović, "Fully Integrated Electronic-Photonic Ultrasound Receiver Array for Endoscopic Imaging Applications in a Zero-Change 45nm CMOS-SOI Process," *2021 Symposium on VLSI Circuits*, 2021, pp. 1-2, doi: 10.23919/VLSICircuits52068.2021.9492412.
- P. Zarkos, S. Buchbinder, C. Adamopoulos, O. Hsu, **S. Madhvapathy**, J. Whinnery, P. Bhargava, and V. Stojanović, "Monolithically Integrated Electronic-Photonic Ultrasound Receiver Using Microring Resonator," in *Conference on Lasers and Electro-Optics*, OSA Technical Digest (Optical Society of America, 2021), paper STh1H.2.

Experience

SOC Power Grid Integrity Intern, *Apple* *June 2021 – August 2021, June 2020 – August 2020*

- Built a scalable data analytics/machine learning framework for SOC power grid integrity analysis

Hardware Engineer Intern, *Ayar Labs* *May 2019 – August 2019*

- Designed, validated, and simulated analog and digital circuit blocks for a clock distribution network in Cadence Virtuoso using Ayar Labs' Python-based Arbitrary Cell Generator (ACG) to automate layout and schematic generation
- Developed ACG infrastructure to simplify differential pair, bus, and ground-shielded routing for open-source use

Hardware Engineer Intern, *MuMec* *September 2017 – May 2019*

- Implemented and tested an FSK demodulator on an FPGA with Verilog and Xilinx ISE that uses frequency mixers for channel selection, digital FIR bandpass filters for bit selection, and lowpass filters for removal of unwanted signals and envelope detection
- Set up ADC and DAC interfacing for measurement and testing purposes
- Designed multiple PCB layouts for measurement boards and a DAC daughterboard using Altium Designer

Software Engineer Intern, *SunPower* *June 2017 – August 2017*

- Conducted economic modeling in Python for residential solar-plus-storage systems using software company Genability's tariffs APIs; simulated customer savings after potential changes to time-of-use rates
- Provided potential policy and go-to-market strategies to provide customers and SunPower with maximum profit

EECS 16A Course Staff, *UC Berkeley* *January 2017 – June 2020*

- Head TA *(Aug 2019 – June 2020)*: monitored and organized student logistics and accommodations, led biweekly discussion sections, and developed exam content in EECS 16A, a course that covers analog circuits and linear algebra
- Discussion/Content TA *(Aug 2018 – May 2019)*: led discussion sections, wrote exam/homework problems, and answered questions in office hours
- Monitored and answered student questions on the EECS 16A Piazza, the course's official online discussion forum

Academic Honors and Awards

NSF Graduate Research Fellow *2022 – Present*

EECS Excellence Award - Funding award for incoming PhD students with an outstanding academic record *2021 – 2022*

EECS Outstanding TA Award - Nominated by faculty and selected by the EECS Student Awards Committee *2020 – 2021*

Member of the EECS Honors Society, HKN Mu Chapter *2017 – Present*